Physics 33228: Spring 2010

Electronics

Lab Manual

Contents

1 DC Elements and Measurements

Reference Reading: Chapter 1, Sections 1.3, 1.4, 1.5 and 1.6.
Two lab periods will be devoted to this lab.
Goals:

1. Become familiar with basic DC ("direct current": zero frequency or constant bias) elements, measurements, and responses.

2. Become familiar with I-V curves for several (linear and non-linear) elements we will use throughout the semester.

3. Become familiar with power computation and the power limitations of real devices.

4. Be able to replace a circuit element with a "Thevenin equivalent" circuit which has the same I-V curve.

5. Test the basic circuit theory of linear devices developed in class and the textbook, most importantly, the voltage divider equation and Thevenin's theorem.

1.1 Introduction

The electrical current, I, through a circuit element is almost always related to electric fields resulting from the application of a voltage, V, across the circuit element. The potential energy difference across the circuit element for a charge Q is just QV. Increasing V across a device corresponds to increasing the average electric field inside the device. The actual electric field inside the device may be highly non-uniform and depend on the arrangement and properties of the materials within the object. However, the behavior of a circuit element within a circuit is generally determined by the relationship between I and V without detailed knowledge of the actual electric field. In this lab, you will study the relationship between I and V for a variety of devices.

The "I-V curve" of a circuit element or device may be obtained in the following manner. First, the element is connected to an external power source such as a variable voltage power supply. Next, the current *through* the device, I, and the voltage *across* the device, V, are measured. The external power supply is then varied so I and V are changed and the new values are measured. This procedure is repeated and the points are plotted on a graph of I vs V. The curve which connects these points is called the I-V curve for the device being tested.

"Linear" devices have I-V curves that are straight lines. For many devices, the "response" or current through the device is proportional to the "input" or voltage across the device over a broad range and their I-V curves obey Ohm's law:

$$V = IR. \tag{1}$$

Devices which obey Ohm's law are called "resistive" elements. Other elements may have non-linear I-V curves or response. In some cases the response is not even symmetric about zero voltage (the response depends on the polarity of the applied voltage).

For direct current, power dissipation can always be written as

$$P = VI. \tag{2}$$

This is just the potential energy change per charge (V) times the amount of charge per second (I) passing through. For resistive elements, this reduces, using Ohm's law, to

$$P = VI = I^2 R = \frac{V^2}{R}. \tag{3}$$

Any of these forms can be used for resistors – choose the most convenient for your purposes. For non-linear devices, you have to use (2).

1.2 Procedure

1.2.1 I-V (current-voltage) curves of *passive* circuit elements

A passive element is a two-contact device that contains no source of power or energy; an element that has a power source is called an "active" element. In the first part of the laboratory, you are to measure and plot the current vs. voltage curve for various passive circuit elements. You are also to plot the power dissipation in each element vs. applied voltage.

You need to decide which of the circuit elements are resistive and which are not resistive. For those elements which are resistive, determine the resistance, R. To do these measurements, you will connect the device under test to a variable voltage power supply and measure I and V as you vary the voltage control of the power supply. Use the circuit shown in Fig. 1.

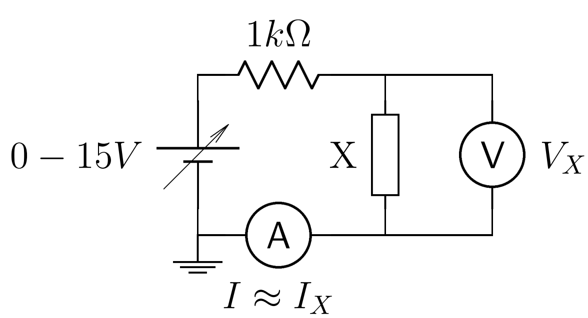

Figure 1: The setup for measuring the IV curve for a passive element, X. The objects labeled A and V are ammeters (ampere-meters) and voltmeters, respectively. The voltage supply is a *variable* one with a range from 0 to 15 Volts.

In this first lab, your first challenge is to correctly wire these circuits on the "proto" board at your station. If you haven't done this before, have the instructor check your wiring before switching on the power supply. Make a table of all your data points and plot them as you go along. Reverse the polarity of the applied voltage by reversing the orientation of the element; this allows you to do measurements from -15 to +15 volts on the supply.

Use the circuit of Fig. 1 to measure the I-V curves and the power dissipation of the following elements. When making these measurements, record the *Applied Voltage* from the supply, the voltage *across the device* from the volt meter, and the *current* through the device.

- 10kΩ resistor
- 1kΩ resistor
- 47Ω resistor
- "7V Zener diode"
- "low current LED"
- light bulb (replace the 1k resistor in Fig. 1 with 100 Ω)

Make plots **(i) by hand, (ii) in your lab notebook, (iii) as you take the data!** Think about the order in which you will take data points **before** you start – in order to plot as you go, you need to know what scale to use for your the axes! Should you start at zero volts? Add plots of the power dissipation vs. applied voltage. You might want to put your data into computer files and have Excel (or some such) compute the power dissipation – *just make sure your results are sensible – powers with "micro-" or "mega-" in front of them just won't do!*

1.2.2 I-V (current-voltage) curves of *active* circuit elements

The I-V (*load curves*), curve of active circuit elements, such as batteries and power supplies, can be obtained by connecting the elements to an external circuit consisting of a single variable resistor. A circuit for measuring the I-V curve of active elements is shown in Fig. 2. A circuit connected to a power source is often called the "load" on the power source and in this case the single resistor, R_L, is called the *load resistor*. As you will see, a *big load* (that is, a *small* resistance) tends to *load down* the source.

> *Think about this language: what's* big *about connecting a small resistor?*

The I-V curve is obtained by varying the load resistor R_L to obtain a set of (I, V) points to plot on a graph. You must find a suitable range of values for R_L so that you get a range of values for I and V. If all your values of R_L are too large, V will vary only a tiny amount; if R_L is too small, the total power V^2/R could exceed the power limitations of the resistor.

Any circuit with two output terminals can be considered as a source. It can be a battery, a power supply, two terminals on the outside of a black box. It does not matter. What does matter is that there is an I-V curve for the source, and there are probably many circuits that give the *same* or *equivalent* I-V curves.

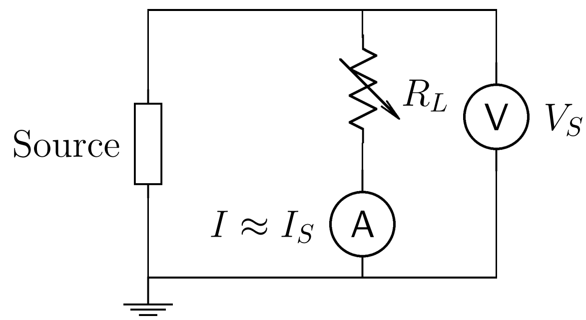

Figure 2: The setup for measuring the *load curve* of a power source. The objects labeled A and V are ammeters (ampere-meters) and voltmeters, respectively. The resistor with the arrow through it is a variable resistor, or a *potentiometer*.

Use the circuit shown in Fig. 2 to measure the I-V curves and power output of the devices listed below. For parts 1 and 2 use a 1 kΩ potentiometer for R_L. In part 3, us a $10k\Omega$ potentiometer for R_L.

1. battery
2. a "50 mA current source" circuit: set up your power supply as follows
   (a) with an open circuit at the output terminals, set the voltage knob to 10V,
   (b) turn the "current limit" knob to zero,
   (c) attach a 10 Ω resistor across the output terminals, and then
   (d) set the "current limit" knob to 50 mA;
   (e) remove the 10Ω resistor and use the output terminal as the "source" in Fig. 2.
3. the voltage divider network shown in Fig. 3 using $R_1 = R_2 = 1$ kΩ and $V = 10$V.

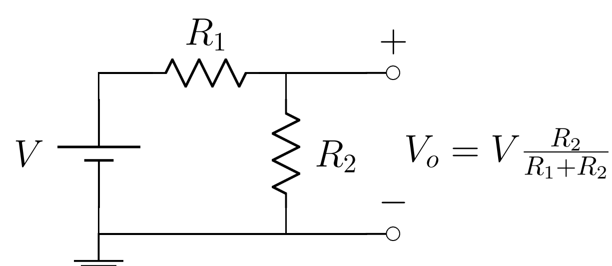

Figure 3: *Voltage Divider Circuit for use in part 3.*

We will find it useful to be able to mimic the behavior of source circuit elements with an *equivalent circuit* consisting of either 1) an ideal voltage source in series with a resistor (Thevenin equivalent circuit), or 2) an ideal current source in parallel with a resistor (Norton equivalent circuit).

What are the Thevenin and Norton equivalent circuits for each of the active devices you investigated above?

1.2.3 The R-2R ladder or current divider

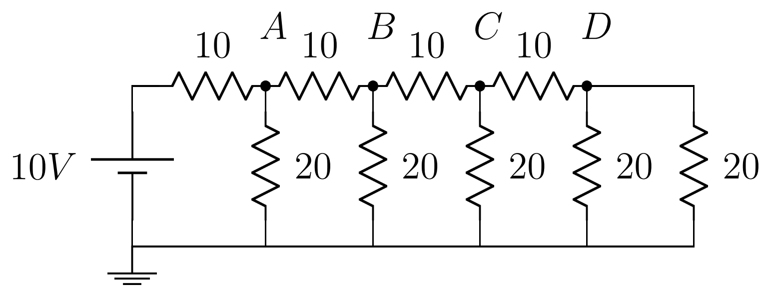

Figure 4: An $R-2R$ resistor ladder. In this diagram, 10 stands for $10\text{k}\Omega$ and 20 for $20\text{k}\Omega$.

The type of circuit shown in Fig. 4 is used in digital-to-analog conversion (DAC), as we will see later in the semester. For the present, it is an interesting example of a resistor network which can be analyzed in terms of voltage and current division and, from various points of view, in terms of Thevenin equivalents.

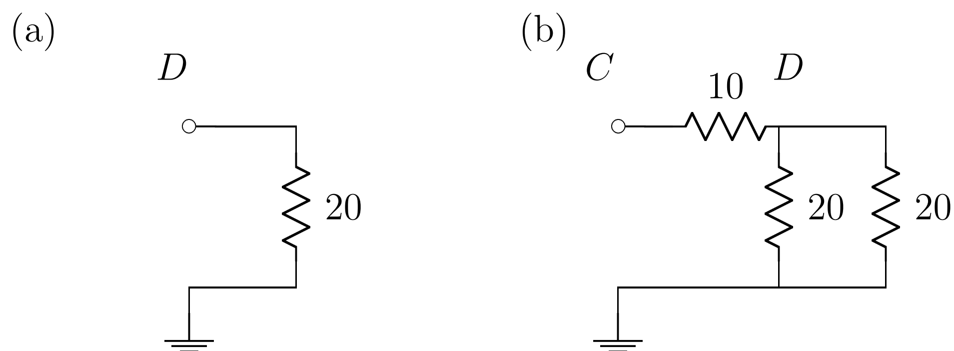

Figure 5: (a) shows the circuit to measure the resistance R from D to ground. (b) shows the circuit to measure the resistance R from C to ground.

We are going to study the properties of this network as we build it. It will be useful to collect all the parts that you need to construct this network using 1% metal-film resistors, but **do not** build it until you have read through the remainder of this section. **If you are so foolish as to ignore this warning, you will find that you need to dismantle the network to make your measurements!**

1. Start by simply putting a $20\text{k}\Omega$ on the board as shown in Fig. 5a. Measure the resistance from the point D to ground. We refer to this as looking to the right into the load.

2. Now add the resistors as shown in Fig. 5b and measure the resistance looking to the right into the load (C to ground).

3. Continue to add pairs of resistors and measuring the resistance looking into the load, (B and A to ground)

4. Add the final pair of resistors and measure the resistance between the terminals to which the voltage source will be connected.

You should now have the resistance network (without the voltage source) on your protoboard using 1% metal-film resistors. These resistors should all be within 1% of their nominal values (that is, the stated tolerance is the maximum deviation, not a standard deviation); the better the precision, the better the network that can be constructed. Show by calculation in your notebook that the results from above are as expected.

Calculate what you expect for the above measurements and compare them with what you have observed. Draw the equivalent circuit that the voltage source will see once it is connected to the resistor network that you built.

5. Now connect the $10\,V$ source and measure the voltage to ground from points A, B, C and D.

Show that these are in accord with expectations. Compute the current and power drawn from the source.

Lets think about extending the network to an infinite number of resistors in the chain.

If we were to do this, what would the equivalent resistance of this network be?

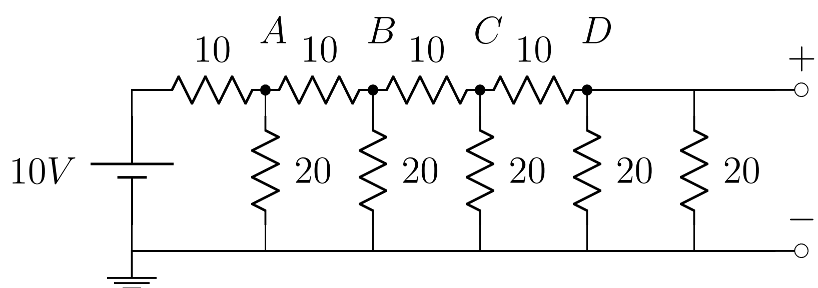

Figure 6: An $R - 2R$ resistor ladder. In this diagram, 10 stands for $10\text{k}\Omega$ and 20 for $20\text{k}\Omega$.

Let us now consider our network as shown in Figure 6 where we connect two outputs at the end of the circuit. It would be useful to know the Thevenin equivalent circuit looking from these new output terminals back toward the source.

Sketch the Thevenin Equivalent for this circuit in your lab book.

6. We can now determine V_{th} and R_{th} of the equivalent circuit. You can measure the open circuit voltage by measuring the voltage from + to −. The equivalent resistance could then be determined from the short circuit current, for example by putting an ammeter between + and −. yAlthough it is safe in this case, this is generally a dangerous procedure.

Why is this procedure considered dangerous?

7. To illustrate a common practical way to determine the equivalent resistance of a source, do the following: Place a known resistance, with a value of the same order of magnitude as the expected equivalent resistance, from + to −. By comparing the voltage across this test resistor with the open circuit voltage, the value of the Thevenin equivalent resistance, R_{th}, can be determined.

   Draw the relevant Thevenin equivalent circuit for this measurement in your notebook and determine R_{th}. How does the predicted short-circuit current compare to what you found by connecting an ammeter from +-to-−? Why is it safe to measure the short circuit current with this circuit?

A conclusion you should assimilate from this part of the lab is that one complicated circuit (for example, the ladder) can be thought of from many points of view – many terminal pairs. For each pair of terminals, there is an equivalent circuit that would mimic the behavior of those terminals. There is no *equivalent circuit* for the entire circuit, but only for specific pairs of terminals. Knowing the equivalent for a pair of terminals makes it easy to think about what will happen to something you want to connect to those terminals. We will use this concept throughout the course!

2 Oscilloscope and Signal Generator Operation

Reference Reading: Chapter 2, Sections 2.1, 2.2, 2.3, 2.4 and 2.5.
Two lab periods will be devoted to this lab.
Goals:

1. Become familiar with the operation of the Stanford Research Systems DS335 signal generator and the Tektronix TDS 2012B oscilloscope.

2. To become familiar with the various ways of characterizing waveforms: rms vs. peak-to-peak amplitude, period vs. frequency content of periodic signals.

3. To optimize data collection techniques for measuring the frequency response of circuits.

4. To become acquainted with frequency response or Bode plots.

5. To become acquainted with the terminology of decibels as used in standard electronic (and other) applications.

2.1 Introduction

This Lab is designed to help you gain familiarity with the Function Generator and the Tektronix oscilloscope you will be using throughout the semester.

The **DS335 Synthesized Function Generator** generates a variety of periodic waveforms of different periods and amplitudes. This is a precision function generator with a highly stable clock for generating signals with different periods. As the name implies, it digitally synthesizes its waveforms in much the same way that a CD player can synthesize signals (the information for which is stored in digital form) that eventually are heard as sound.

The **Tektronix TDS 2012B oscilloscope** provides a means of observing these and other periodic waveforms. Very briefly, a digital oscilloscope emulates an analog oscilloscope which images a periodic waveform by repeatedly passing a dot (the position at which an electron beam hits the phosphor screen of a cathode ray tube) across a screen at a sweep rate (the rate of passage across the screen) and repeat rate (usually determined in various ways to generate a repeating pattern) appropriate for the signal being observed. Thus, the horizontal axis is time and the vertical axis is the voltage being measured. You can directly select the sweep rate and the scale factor for the vertical axis. The trickier part is to arrange to have the sweep repeated in such a way as to generate the same picture of the waveform on each sweep – otherwise, you see a confusing jumble on the screen. As described below, the sweep can be "triggered" in several different ways.

Taking data. *Note: This discussion applies both the this lab and to several labs later in the semester.* Both the signal generator and the oscilloscope operate over several decades in their key parameters: waveform amplitude and frequency. Not coincidentally, analog circuits must operate properly over a similar range of signal parameters and you will need to both characterize *and display* such behavior. The measurements are straightforward enough given the matched scales of the instruments.

For properly displaying circuit behavior over several decades, a linear scale plot fails miserably. However, a base-10 logarithmic scale gives equal space to each decade or factor of 10 (actually, any base will do the same trick, but base-10 is conventional because of its simple powers-of-ten convenience). In this and subsequent lab exercises, you will want to select where you take data points (primarily at what frequencies) so that the points uniformly fill several decades on a log scale. If you want n points per decade, you'd choose $10^{1/n}$ and integer powers thereof. For example, in frequency measurements with $n = 1$, you could take data at, for example, 1Hz, 10Hz, 100Hz,... or 5Hz, 50Hz, 500Hz,... . For $n = 3$, 1Hz, 2.15Hz, 4.62Hz, 10Hz, 21.5Hz,... could be used. When viewed over several decades, great precision is generally not necessary, so it is common to see 1Hz, 2Hz, 5Hz, 10Hz, 20Hz... used. You might also want to take note of the resistor values available (from about 1Ω through 10MΩ – covering seven decades) in the laboratory – and from manufacturers.

2.1.1 Using the DS335 synthesized function generator

The controls for the DS335 are in three groups:

1. Buttons on the left control what is displayed: either the frequency, amplitude or the DC offset.

2. The center buttons (FUNC) control the form of the output waveform.

3. To the right is the DATA ENTRY section with a numeric keypad and increment buttons. The SHIFT key accesses the functions located above the numeric keys and the arrow keys below.

4. On the lower right is the POWER button and STATUS lights which, for our purposes, indicate when you input something the generator doesn't understand or can't do.

The controls are summarized below; you should experiment to become familiar with these:

1. Upon power-up, the display cycles through a start-up procedure; wait for the default display to appear. Pressing SHIFT and INIT in the DATA ENTRY section puts the device into a default configuration: the output is a sine wave at 1MHz, 2V peak-to-peak ($2V_{pp}$), with no offset (the amplitude will read $1V_{pp}$ because the default "load impedance" is 50Ω – see section 4 below).

2. The default waveform is a sine wave. To change, toggle the FUNC button through square, triangular, sawtooth, and noise, then back to sine.

3. *To change frequency*: As you know from Fourier analysis, only a sine wave is composed of a single frequency component. Nevertheless, it is convenient to specify all the selectable waveforms by a single "frequency" designation. This frequency is really the inverse of the fundamental period (the repeat period) of the wave. Non-sine wave signals contain this

frequency as well as higher order harmonic components at multiples of the fundamental frequency.

Two methods are available for setting the frequency:

1. With the FREQ displayed, enter a number, then hit either MHz, kHz, or Hz to specify the intended units; or

2. With FREQ displayed, you will notice that one of the displayed numbers is blinking. Press the Vpp/kHz "up" button and see that the blinking number is incremented upwards by one. Pressing SHIFT and → or ← will shift the blinking digit so you can increment in larger or smaller amounts.

4. *To change amplitude*: The same two options are available as under FREQ mode. Note that you can specify the amplitude in two different units and with two different modes:

1. In Vpp mode, you enter the peak-to-peak excursion of the output voltage. This works for any waveform.

2. In Vrms mode, you enter the root-mean-square voltage. Only use this mode for sine wave signals.

The Thevenin equivalent resistance of the DS335 signal source is 50Ω. That is, the output of the generator "looks like" an ideal voltage (signal) source in series with a 50Ω resistance. The reading of the output display can be changed from "High Z" to "50Ω" with switches in the DATA ENTRY section. The intent of this toggle is to allow you to display the actual voltage delivered to your load under the conditions that the load is i) much larger than 50Ω ("High Z" setting) or, ii) *equal* to 50Ω ("50Ω" setting). If you have a load which does not satisfy either of these conditions, you should use the "High Z" setting and compute and/or measure the voltage delivered to your circuit. **Toggling the reading does not change the output of the generator in any way!**

5. *DC level*: One can superimpose a DC level on an AC signal:

1. Set up the desired AC signal.

2. Press OFFS

3. Enter the DC offset voltage in data entry.

Using this, you can, for example produce a square wave where the low voltage side is at zero instead of a negative voltage; this will be useful for digital circuits.

6. *Frequency sweep*: The DS335 can repeatedly sweep its frequency over the entire range of its output or any fraction thereof at a rate selected by the user. The sweep can cover frequencies at either a linear or a logarithmic rate. To set up a sweep, follow these directions:

1. Reset to default settings.

2. Set the desired amplitude.

3. Press the SHIFT key, then the STOP FREQ/LIN/LOG key. The display should read **Lin.Lo9**, with the first **L** blinking indicating a linear sweep rate. You can toggle this with the → and ← buttons.

4. Press SWEEP RATE, then enter the inverse of the desired sweep time (i.e., 0.5 Hz for a 2 second sweep through the selected frequency range).

5. Press the START FREQ key and enter the desired starting frequency.

6. Press the STOP FREQ key and enter the stop frequency.

7. To start the sweep, press SHIFT, then the START FREQ/ON/OFF key.

The DS335 puts out a trigger pulse once for each frequency sweep, so you can trigger the scope once on each sweep in order to quickly visualize the frequency response of a circuit (you will need to set the scope sweep time to be greater than or equal to the DS335 sweep time).

2.1.2 Using the TDS 2012B oscilloscope

The User Manual for your oscilloscope is available in the lab. Pages 1-36 cover the basic operational details. The chapter on Application Examples shows how to do various types of measurements, several of which are similar to the laboratory exercises. Most features are documented in the instructions under the HELP button, which you can search via the index or by simply pressing 'HELP' after pressing a button about which you would like to learn. Below are a few notes to help orient you.

The TDS 2012B is more than a traditional oscilloscope. The latter would simply show a waveform as it occurs in a circuit. The TDS 2012B is a *digital scope*: it digitizes the waveform and can store a single waveform so that you can analyze it after it occurs. Like a 'storage scope', it will display on its screen indefinitely the last trace for which it was triggered. (Warning: This means you may be fooled into thinking the scope is seeing something when it is really displaying an old waveform! In particular if you press the RUN/STOP button, the scope won't run normally until you press it again. STOP lights up in red at the top of the screen to warn you if the 'scope has been stopped.) Of course, the scope can also perform the functions of a traditional real-time oscilloscope. The scope can save waveforms to floppy disks so you can do further analysis on a computer. The scope performs a variety of analyzes of waveforms (amplitude, period,...) and can do so in a continuous way, constantly updating the results. You will use this capability extensively. Some measurements (in particular, comparisons of different waveforms) require you to manipulate the cursors and read off values of various quantities.

The controls for the scope are a combination of front panel knobs and menus displayed on the screen. Getting familiar with both of these is one of the main points of this lab.

- You select input channel 1 or 2 with the two buttons so-labeled (yellow and blue). After pressing one of these, you can change the settings for the corresponding channel. (Each channel has dedicated control knobs for vertical scale and vertical position, regardless whether that channel is selected or not.) Note that pressing a channel menu button when that channel is already selected turns off the display of that channel. Pressing again turns it back on.

- **VERTICAL** section: The scale of the vertical axis is controlled by the **VOLTS/DIV** knob. The calibration, in volts per large grid unit, is displayed on the screen. You can move the zero volt point with the "position" knob.

  Notice that the vertical scale for each channel is displayed on your scope screen (in volts per division).

- **HORIZONTAL** section: The scale of the horizontal axis (time) is controlled by the **SEC/DIV** knob. The calibration, in time per large grid unit, is displayed on the screen. You can move the track horizontally with the "position" knob.

  Notice the scope screen always displays the time scale (in time per division).

- **TRIGGER** section: The triggering of the sweep is controlled by this section. When trying to visualize a time-varying but periodic voltage (e.g. a sine wave), the scope needs to start its sweep at the same point on the waveform each time – otherwise, you will just see a jumble of lines on the screen. By starting at the same point, you get a stable pattern. The **LEVEL** button controls the voltage level at which the sweep will begin. Note that, if this level is outside the range over which your input signal varies, the scope never triggers! (Or, in AUTO trigger mode, it will trigger randomly!) Several other controls are on the Trigger menu screen, accessed by pressing the Menu button. The **SLOPE** control determines whether the sweep begins when the input crosses the trigger level while rising(increasing in voltage) or while falling (decreasing in voltage). The **SOURCE** control decides whether channel 1 or 2 is tested for the trigger condition. (Or whether the EXT TRIG input, or the *power line* is used to trigger the scope.)

  Notice that the scope screen (on the bottom right) shows which channel it is triggering on, whether it is looking for a rising or falling slope, and a what level it will trigger. (It also displays the frequency at which it is being triggered.)

- In the **Vertical**, **Horizontal** and **Trigger** and sections are **MENU** buttons that bring up on-screen displays with expanded sets of options.

- One important button is the **AUTOSET** located on the right side of the top row. This generally sets the scope parameters so that the input signal will appear on the screen. When all else fails, try this! (But, generally, Prof. Quinn hates it!)

- The **ACQUIRE** button allows you to select 'Sample' mode (which is typically used) or 'Average' mode which can be much more confusing, but is useful for cleaning-up a repetitive signal which has non-repetitive noise on it.

- The **MEASURE** button in the top row allows you to set up a variety of types of automatic measurements. Some measurements you will want to use include: the **Frequency** and **RMS** (which is usually more reliable than peak-to-peak which is more noise sensitive).

- The **SAVE/RECALL** and **Print** buttons allow you to save (to memories in the scope or to a flash drive) all the settings of the scope and/or a screen image and/or the measured values. If you save the settings, you can then re-adjust the scope for a different job and then return to what you were doing. (Starting next lab, you will use it to save the measured values of the waveform you are looking at. You mustn't confuse these two different ways of using SAVE!) There are also two memories (REFERENCE A and B) which can save a waveform so you can display it on the screen to compare to what you see later.

- The **CURSOR** button turns on vertical or horizontal markers (with their exact positions indicated). These are sometimes useful for making measurements 'by hand' when the automated measurements are not trustworthy. It's always good to check occasionally to make sure the scope isn't giving nonsensical values with its automated measurements.

- The DEFAULT SETUP button will turn off any 'crazy' modes to which the scope may be set (perhaps by the last people who used it).

- The scope probes allow you to test the voltage at various points in a circuit. Notice that the probes have X1 and X10 settings selected by a switch. Be careful to not use the X10 setting (unless you also set the scope to multiply its input by 10) or you will be off by a factor of 10 in the measurements you make.

2.2 Procedure.

1. **Play!** Take notes of what you do and what you see/measure with the scope as you do this. Visualize each type of waveform from the DS335 on the oscilloscope. Adjust frequency, amplitude and DC offsets and observe the resultant waveforms. Be sure to try the different input coupling settings (DC or AC set using the channel menu buttons) on the scope as you change things like the DC offset. (*It will be important to keep track of the setting of the coupling*, especially when measuring at low frequencies or for signals which don't average to zero. Usually you want the coupling set to 'DC'... except when you don't.) Try (using the *Trigger* menu) triggering internally and externally using the SYNC OUT from the DS335. Make sure that you understand the function of the "High Z" - "50Ω" switch on the DS335. You will need to explain this to one of the instructors.
   Try saving you scope settings, messing things up and then recalling the saved settings.

   You probably can't trust the amplitude reading of the DS335. Often the most accurate measure of size of a signal is the one found "by hand" by positioning the scope's *horizontal* cursors where you best estimate the top and bottom of the signal to be. You can also tell the scope to make automated measurements of Pk-Pk (Peak-to-peak size) and RMS.

Note: You will always get the best accuracy from the scope if the vertical and horizontal scales are adjusted so one cycle of the waveform fills most of the screen! In general, don't forget to adjust your scope whenever the waveform starts to look small.

Compare all of these measurements to your "hand" measurements for sine, square, and triangle waves. Which automated measurements are the most accurate? What does the RMS voltage setting mean when applied to sine, square or triangle waves? Compare calculated RMS values to the waveforms you observe.

2. **A Voltage Divider.** Build a voltage divider with $R_1 = 100\,k\Omega$ and $R_2 = 2.2\,k\Omega$. Measure the exact values of your two resistors so that you will be able to make accurate predictions. Now set your DS335 to a sine-wave output with a frequency in the range 100 kHz to 1000 kHz. Set the output voltage to be $0.75\,V$ peak-to-peak. Connect this voltage across your divider, and then connect channel one of your scope across the entire divider. Use the scope, set to $1V/division$, to measure the *RMS* and *Peak-to-Peak* voltage.

   Are these consistent with the output of your signal generator? Measure the peak-to-peak voltage by hand (using the cursors) and compare to the previous measurements.

   Now adjust the scope to have $0.1\,V/division$ and repeat your measurements.

   Connect channel two of the scope across R_2. Based on what you measured earlier, predict what you should measure on channel 2. Make the measurements and compare them with your predictions.

   Which method is the most accurate? What problems do you encounter in your measurements?

3. **Frequency response of the R-2R ladder circuit.** Substitute the DS335 for the DC voltage source in the R-2R ladder circuit of Laboratory 1 (be sure to include the final 20kΩ resistor). Select a $10V_{pp}$ sine wave with zero offset voltage (check with the scope to be sure this is what you've got). Measure the amplitude of the voltage at point D as a function of frequency over the range 1Hz to 3MHz. As discussed in the introduction, take data so that when you make a plot with a logarithmic frequency scale the points are roughly equally spaced. To verify that the frequency dependence you observe is not a result of a variation in output of the DS335 or sensitivity of the scope, use both scope channels with one directly connected to the DS335 output. Be sure to use DC coupling of the input signal on both channels.

Make a *Bode plot* of the measured frequency response. This is a log-log plot of the relative gain ($V_{out}(f)/V_{ref})$) vs. frequency, where V_{ref} is a chosen reference voltage. In this case, use $20\log_{10}(V(f)/V(1000\text{Hz})$ for the vertical axis and $\log_{10}(f)$ for the horizontal axis. The vertical axis is referred to as a "decibel" or "dB" scale – it is a standard in electronics.

A 'bel' (named for Alexander Graham Bell) is a factor of 10 change in **power**. This is commonly used to measure quantities such as amplification and attenuation. For example, the amplification, in bels, is $A_{\text{bel}} = \log_{10}(P_{\text{out}}/P_{\text{in}})$. Then, since $P \propto V^2$ for resistive loads, we have $A_{\text{bel}} = \log_{10}((V_{\text{out}}/V_{\text{in}})^2) = 2\log_{10}(V_{\text{out}}/V_{\text{in}})$. Then a decibel is a tenth of a bel, so the numerical value of the amplification in decibels is ten times more than it is in bels, so $A_{\text{decibel}} = 20\log_{10}(V_{\text{out}}/V_{\text{in}})$.

On a frequency response plot, the "characteristic frequency" is that frequency at which the response falls to $\sqrt{\frac{1}{2}}$ (about 0.7) of its nominal or reference value. Remembering that the power delivered to a resistor goes like V^2, this point corresponds to where the power delivered is reduced to $\frac{1}{2}$ that at the reference frequency. Since $\log_{10}(0.7) \approx -0.15$, the vertical scale in the Bode plot is down by 3 dB and this frequency is referred to as a "-3 dB point". *Note the -3 dB frequency on your plot.* Also (if you have sufficient data range) determine the rate of fall-off of the frequency response in dB/decade (this is called the "roll-off" rate).

> *If the response falls at a rate of α dB/decade, what does this imply about the functional form of $V(f)$?*
>
> *Is the high frequency behavior what you expect for a device made entirely of resistors? Can you explain what might be happening?*

4. **AC vs. DC coupling into the oscilloscope.** When an input channel is set to "AC coupling", an input blocking capacitor is put in series between the input terminal and the scope's amplifier. This capacitor will reduce the scope's response at low frequency (we will consider this effect quantitatively in a later lab); the input gain is zero at zero frequency or DC. This blocking function is convenient when you want to examine a small AC signal that rides on top of a larger DC offset.

   By putting the same signal into both channels of the scope and coupling one AC and one DC, measure the frequency response of the AC coupled channel of the scope. At high enough frequency, both channels should yield the same trace – you can overlap the traces so you can see when they start to deviate. Starting at a "high" frequency, measure the frequency response of the two channels and make a Bode plot using the ratios of the two measured signals. Determine the -3 dB point and the roll-off rate.

   You will need to remain aware of these results when you do measurements throughout the rest of the semester. You'll have to choose whether to use AC or DC coupling for each measurement.

3 RC and RL circuits: Time Domain Response

Reference Reading: Chapter 2, Sections 2.6, 2.7 and 2.8.
Two lab periods will be devoted to this lab.
Goals:

1. Characterize the exponential response to step inputs of reactive circuits.
2. Come to terms with the meaning of a "characteristic time": $\tau = RC$ or $\tau = L/R$.
3. Understand two rules of thumb:
   (a) One cannot instantaneously change the voltage across a capacitor.
   (b) One cannot instantaneously change the current through an inductor.

3.1 Introduction

We introduce two new circuit elements in this laboratory: capacitors and inductors. Together with resistors, these complete the list of two-terminal, linear devices which are commonly used in electronics.

In this and the following lab, we will study circuits with various combinations of resistors, capacitors, and inductors from two different points of view: the *time domain* and the *frequency domain*. In the time domain we examine transient responses to sudden changes in applied voltages (the closing of a switch or the application of a step change in voltage). In the frequency domain, we will study the response to sinusoidal applied voltages as a function of frequency. The two points of view turn out to be entirely equivalent: complete knowledge of the behavior in one domain implies (with appropriate theory) complete knowledge of behavior in the other. Both points of view are useful throughout electronics as well as being applicable to a wide variety of other physical systems.

3.1.1 RC circuit analysis

The voltage across a resistor-capacitor pair wired in series (see Fig. 7) must equal the voltage across the capacitor plus the voltage across the resistor. If we write the voltages as a function of time (as opposed to functions of angular frequency ω), then we are using a *time domain* treatment of the problem. The equation for the voltages in the RC circuit is

$$v(t) = v_C(t) + v_R(t). \tag{4}$$

Using the relations $v_C = Q/C$ and $V_R = i(t)R$, this can be rewritten as:

$$v(t) = Q(t)/C + i(t)R. \tag{5}$$

$Q(t)$ on the capacitor and $i(t)$ in the circuit loop are related by

$$Q(t) = \int_0^t i(t')dt', \tag{6}$$

assuming $Q(0) = 0$, or

$$i(t) = \frac{dQ}{dt}. \tag{7}$$

Combining (6) or (7) with (5), a variety of interesting limits can be found. For example, by taking the derivative of (5), we can express the right side in terms of a single time varying quantity, $v_R(t)$:

$$\begin{aligned} \frac{dv}{dt} &= i/C + R\,\tfrac{di}{dt} \\ &= v_R \tfrac{1}{RC} + \tfrac{dv_R}{dt}. \end{aligned}$$

If the voltage across the resistor changes slowly enough we can neglect the second term on the right: $\frac{dv_R}{dt} \ll \frac{v_R}{RC}$ or $\frac{1}{v_R}\frac{dv_R}{dt} \ll \frac{1}{RC}$. Referring back to (5), this amounts to requiring the voltage on R to be small, so most of $v(t)$ appears across C. Finally, we get

$$v_R(t) = RC\frac{dv}{dt}. \tag{8}$$

For slowly varying signals, the voltage across the resistor is proportional to the derivative of input voltage. This is called a differentiating circuit – it will differentiate slowly varying input voltages.

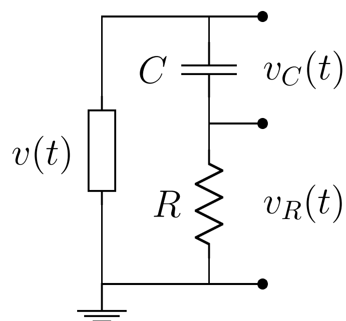

Figure 7: An A.C. source driving a simple RC circuit

Note that the quantity $\tau \equiv RC$ has the units of time. This is the *characteristic time constant* **of an RC circuit. This is another quantity that will arise again and again!**

One can also take the integral of equation (5) to get:

$$\int_0^t v(t')dt' = \frac{1}{C}\int_0^t Q(t')dt' \;\; + Q(t)R. \tag{9}$$

Looking back at (5), we see that as long as the voltage on C is small, we can neglect the first term on the right. This means that $\frac{Q(t)}{RC} \ll i(t) = \frac{dQ}{dt}$ or $\frac{1}{i}\frac{di}{dt} \gg \frac{1}{RC}$ – i.e., the signal should be rapidly varying. Dividing (9) by RC,

$$v_C(t) = \frac{1}{RC}\int_0^t v(t')dt'. \tag{10}$$

For rapidly varying input signals, the voltage across the capacitor is the integral of the input voltage, $v(t)$.

3.1.2 Analysis of RL circuits

The voltage across a series wired inductor-resistor pair can be written as:

$$v(t) = v_L + v_R = L\frac{di}{dt} + iR. \tag{11}$$

Analysis similar to that above for the capacitor yields integrator and differentiator circuits:

- For slowly varying inputs, most of the voltage is across the resistor and the remaining voltage across the inductor satisfies

  $$v_L(t) = \frac{L}{R}\frac{dv}{dt}. \tag{12}$$

  Dimensional analysis implies that $\tau \equiv \frac{L}{R}$ is the characteristic time constant for this circuit.

- For rapidly varying inputs, most of the voltage is across the inductor and

  $$v_R(t) = \frac{1}{\tau}\int_0^t v(t')dt'. \tag{13}$$

3.2 Procedure

3.2.1 Time domain response of RC circuits

Voltage across the resistor. Investigate the output characteristics of the circuit shown in Fig. 8. In order to observe the complete transient response, you want to apply a step voltage and then hold this applied voltage for a time that is long compared to τ (i.e., until the transient has died away). A 'transient' is a temporary signal which exists as a system moves from one stable mode to another. In this case, the transient exists as the system moves from an uncharged capacitor and zero applied voltage to an applied voltage and a steady charge on the capacitor.

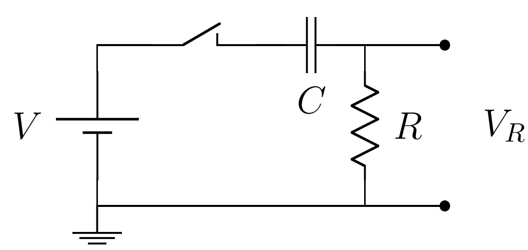

Figure 8: Setup for time response of RC circuits

- Set up the circuit shown using C = 0.33μF and R = 1kΩ.
- As the supply voltage, use 5 Volts from the DC supplies at your experimental station. The diagram indicates that you could ground one point of the circuit. In fact it is more convenient to work with the circuit "floating", meaning that you don't ground any point. Then you can connect the scope leads (one of which is grounded) anywhere in the circuit without introducing an unintended short.
- Calculate the numerical value of the time constant for this circuit.
- Instead of using a switch, you should be able to obtain the transient response by plugging a banana plug into the terminal on your proto-board or just plugging a jumper wire into the protoboard.
- You will have to set up the oscilloscope to take a "single shot" measurement of the transient. This will require some trial and error to make the triggering work and to be sure that you get the horizontal and vertical scales right. Remember that you must discharge the capacitor after each attempt – you can do this by connecting a wire across it for a short time. You can erase trial signals and reset the trigger by pushing the **single seq** button.

  If you have trouble capturing the signal with your scope, you may want to warm up on something simpler. Try to measure the voltage across a resistor just as you apply voltage across the resistor. This gives you a very simple step function to practice triggering your scope.
- Once you have obtained a clean transient signal, you should transfer the data to a diskette so that you can perform least-squares fits on a computer. Be sure to SAVE the wavefunction of interest (not the scope setup and not the wrong channel of the scope) in spreadsheet format. To make sure everything is working correctly, plot *at least* one of your measurements on the computer before going on to do the rest of the experiment.
- Verify that the expected *functional form* and time constant are observed.
  - To verify the functional form, make a plot that will make the expected form a straight line. To do this, note that if

    $$v(t) = Ae^{-t/\tau} \tag{14}$$

    then

    $$\ln v(t) = \ln A - t/\tau. \tag{15}$$
  - The above equation implies a "natural" way to plot your data. Find a way to plot your data so that your data points form a straight line with slope $-1/\tau$. What happens if you use $\log_{10}(...)$ instead of $\ln(...)$ ($\log_{10}$ is a more customary way to plot data because humans have ten fingers instead of 2.7182818...!)?

The input function to your circuit is a *step function* that turns on when you close the switch. When we are looking at the response of an RC circuit, we talk about times either *long* or *short* compared to the time $\tau = RC$.

- *What does the derivative of a step function look like?*
- *What part(s) of the observed output signal mimics the derivative of the input "signal"? Is this consistent with the above equations?*

Voltage across the capacitor.

1. Reverse the positions of R and C in your circuit and measure the transient response across C. Or, if you haven't grounded the circuit you can just move the scope probe leads to the capacitor.
2. Graph and fit the voltage across C as a function of time. Note that the voltage across the capacitor is *not* simply an exponential. So simply taking the ln of your data won't give you a linear graph to fit. Think about what simple manipulation of your data you must do in addition to taking the ln.

The input function to your circuit is a *step function* that turns on when you close the switch. When we are looking at the response of an RC circuit, we talk about times either *long* or *short* compared to the time $\tau = RC$.

- *What does the integral of a step function look like?*
- *What part(s) of the observed output signal mimics the integral of the input "signal"?* (Hint: think about τ).

Measuring a fast transient. To see how well the scope works, try measuring the transient in a circuit with $R = 470\Omega$ and $C = 27$pf (or similar values). *What is the calculated time constant?* Recall that the speed of light is 1 foot per nanosecond (excuse the units!)

You aren't likely to be able to close a mechanical switch fast enough to make these measurements. Instead, you can replace the D.C. power supply and "switch" with the square-wave output of your DS335 Function Generator. This will serve to charge and discharge the capacitor repeatedly. You should use a high frequency square wave. Prove to yourself that the circuit will have many RC times to reach equilibrium before the square wave voltage reverses.

Even the "square wave" can't make transitions on a time scale which is fast compared to RC. Look at the shape of your square wave on the scope and determine how long it takes the voltage to "ramp up" to a resonably stable level. You only expect the simple RC behavior in the circuit once the input voltage has stabalized. When you analize the data, you will want to ignore the first part of the transient, taken when the input voltage was changing. Knowing the "ramp up" time allows you to decide which part of the data to discard.

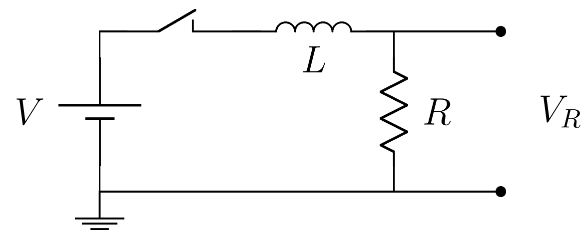

Figure 9: Setup for time response of RL circuits

Again, you should measure, plot, and fit the transient across the resistor and across the capacitor. Now the circuit is not floating because the DS335 output is grounded on one side. You'll have to arrange the circuit so you can measure the desired voltage while still having the ground connection of the scope connected to the same part of the circuit as the ground connection of the function generator.

3.2.2 Time domain response of RL circuits

The circuit shown in Fig. 9 and the one with R and L interchanged are to be investigated. Real inductors introduce a slight complication: they have an internal resistance, R_L, that is generally non-negligible and we have to write

$$v(t) = \left[L\frac{di}{dt} + iR_L \right] + iR. \tag{16}$$

The internal resistance is usually not shown in circuit diagrams, but must always be kept in mind. For example, you cannot directly measure the voltage across *just* the inductance; the apparent voltage is across the series combination of L and R_L. In fact, R_L is not just the DC resistance of the coiled wire either: The effective R_L includes all dissipative effects which remove energy from the circuit. This includes inductive heating in any magnetic core material around which the coil is wound and, at high frequencies, radiative effects as well.

1. Measure the apparent resistance and inductance of your inductor with your Ohmmeter and the LRC meter.

2. Setup the circuit shown in Fig. 9. Use a series resistance (R in the diagram) that has a value comparable to R_L.

3. Measure the functional form and time constant of the voltage across R in the same way you did for the RC circuit. Also, note the final voltage across R. *What are the final and initial voltages across L?*

4. *What is R_L?* There are (at least) two ways to determine this from the data: from the time constant and from the final voltage across R. *Do these agree with each other? Do they agree with our ohm-meter measurement of R_L?*

4 RC, RL, and RLC circuits: Frequency Domain Response

Reference Reading: Chapter 3, Sections 3.1, 3.2, 3.3, 3.4, 3.5, 3.6 and 3.7
Two lab periods will be devoted to this lab.
Goals:

1. Gain familiarity with AC frequency response of simple RC, RL, and RLC circuits:
   (a) Amplitude response.
   (b) Phase response.
   (c) Measurement of above quantities.
   (d) Calculation of above quantities.
2. Come to terms with the meaning of a "characteristic frequency": $\omega_o = 1/(RC)$, $\omega_o = R/L$, or $\omega_o = 1/\sqrt{LC}$ (compare to Lab 3 statement regarding "characteristic times").
3. Understand the meaning of the terms "low pass filter" and "high pass filter" and be able to identify them in a circuit.
4. Understand the requirements for coupling circuit units together in a modular fashion.
5. This lab is an excellent place to compare theory and experiments. Such comparisions are expected in your lab book and you should sketch the theoretical expectations on the same plots with your data.

4.1 Introduction

We now re-examine the circuits of Lab 3 in a different way: we apply sinusoidal waves rather than step inputs. We compute and measure the amplitude and phase (relative to the source) of the output. Your measurements should be compared to quantitative calculations of the expected behavior of the circuits.

The RC and RL circuits in this lab can be modelled as AC voltage dividers. Consider the voltage divider network shown in Fig. 10. If the sinusoidal input to the divider network is written as

$$v(t) \quad = \quad Re\left(V_{in}e^{j\omega t}\right)$$

then the output can be written as

$$v_{out}(t) \quad = \quad Re\left(V_{out}e^{j\omega t}\right)$$

where

$$V_{out} = \frac{Z_2}{Z_1 + Z_2}V_{in}$$

The voltage divider result can also be applied to RLC circuits, with Z_1 being replaced by Z_R and Z_L combined in the appropriate way. The resulting behavior is more complex than RC and RL circuits, in that RLC circuits exhibit resonant behavior at a characteristic frequency, $\omega_o = 1/\sqrt{LC}$. These circuits are discussed in detail in the textbook.

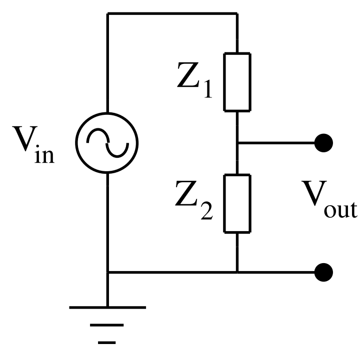

Figure 10: Generalized voltage divider constructed of two components with impedances Z_1 and Z_2.

4.2 Procedure

Reminder: At the beginning of each section below, enter into your lab notebook a summary of what you are setting out to do and what the relevant equations are expected to be. Derivations and great lengths of verbiage are not necessary, but some orienting explanation is. This should be standard practice in any lab notebook!

4.2.1 Frequency response of the *RC* voltage divider.

1. Set up the RC circuit using $C = 0.008\mu$F and $R = 22\text{k}\Omega$ and a sine wave of reasonable amplitude (say, 5 Volts). Calculate the expected characteristic frequency in radians per second and in cycles per second (Hz).

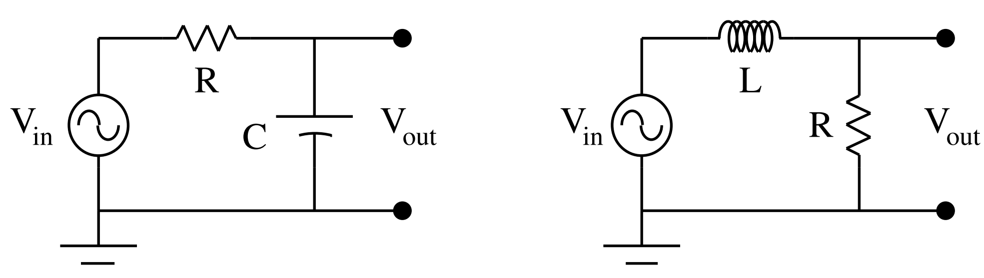

Figure 11: RC and RL circuits

2. For both the integrator and differentiator configuration, make careful measurements of V_{out} and V_{in} over a frequency range that extends at least two decades below and above the

calculated characteristic frequency (be careful about factors of 2π). *As you take the data*, plot the "gain", $|G(f)| = |V_{out}|/|V_{in}|$, on a Bode plot and the phase shift between V_{out} and V_{in} on semi-log scales. (Recall that a Bode plots is $20\,dB \times \log(G)$ versus $\log(f)$.) Set up the scope to display both signals. The scope can be set to measure the amplitudes of each. You can use the cursors to measure phase shift: You calibrate the distance corresponding to 360 degrees, then set one cursor on the zero crossing point of the input signal, the other on the corresponding zero crossing of the output; the ratio gives you the phase shift as a fraction of 360 degrees.

- In one configuration, V_{out} is the voltage across R; in the other, V_{out} is the voltage across C. You must determine the necessary wiring for each case.
- Choose your frequency steps so that your measurements will be equally-spaced on a logarithmic frequency axis.
- Should you be using the scope's AC coupling input mode for this measurement?
- Determine the slope of the Bode plot (dB per decade) in the high or low frequency limit (wherever $G(f)$ is varying). Make a plot of your data together with a theoretical function drawn through (or near?) the data.
- Determine the frequency at which $|V_C(f)| = |V_R(f)|$. Compare your measured value to the calculated value.
- Over what range of frequencies do you expect the circuit to integrate or differentiate the input signal? To figure this out, you can use the analysis in the Lab 3 write-up or use the frequency domain logic in Section 3.4 of the textbook. Use the different waveforms available from the signal generator to see that the proper mathematical operation is performed. Choose an appropriate period for the waves so the integrator or differentiator should work well.

4.2.2 Frequency response of the RL voltage divider.

Repeat the above procedure with the "low pass" configuration of an RL circuit. Use a $2.2\,k\Omega$ resistor for R and measure L and R_L. Which circuit, RL or RC, works better as a low-pass filter? Why?

4.2.3 RLC Resonant Circuit.

Construct a series RLC circuit as shown in Fig. 12. Use your $0.008\mu F$ capacitor and the inductor from the previous part. Study the discussion of RLC circuits given in section 3.5 of the textbook and calculate a predicted resonant frequency, ω_o. You don't need to include any explicit resistance in this circuit: in your analysis, include the source resistance and that internal to the inductor.

Measure the frequency response over the appropriate frequency range. Again, choose frequency steps that will be equally spaced on a logarithmic frequency axis. Make a Bode plot and a phase shift plot as in the above procedures. Compare to the calculated behavior. Use your measurements of the amplitude and phase as functions of frequency to determine the value of the internal resistance of the inductor. Comment on the result.

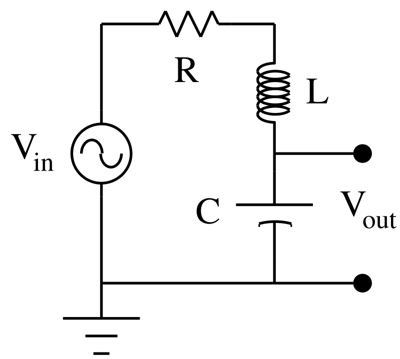

Figure 12: RLC circuit configured to measure the voltage across the capacitor.

4.2.4 Coupling circuits together: a bandpass RC filter.

As discussed in Section 3.7 of the textbook, there are many occasions when we need to couple one functional block of circuitry to another – in fact, it's hard to think of a situation where this is not necessary! Here, you will design a "bandpass" filter circuit by taking the output of a high pass *RC* filter and putting it into a low pass *RC* filter with the same characteristic frequency.

Repeat the design logic of Section 3.7 of the textbook but use a factor of 20 in place of the 100 used there. This leads to more comfortable element values. You should find that you can build the low pass stage of the circuit using the same components you used to build the RC circuit earlier.

Again using 5 Volts from the signal generator, measure the frequency response (amplitude and phase) and compare to the expected response.

What this exercise does not show you (at least if you do the design correctly) is how things go wrong when you do not have the correct progression of input and output impedances. If you have time, you might want to try using $R_1 = R_2$ and $C_1 = C_2$ and see what happens to the response.

5 AC to DC Conversion and Power Supplies

Reference Reading: Chapter 4, Sections 4.5 and 4.6.
Two lab periods will be devoted to this lab.
Goals:

1. Understand the use of diodes to convert AC signals with no DC component into oscillatory signals with appreciable DC components.

2. Understand the use of filter circuits to obtain relatively "clean" DC voltages.

3. Become familiar with the "regulation" of various constant voltage supply circuits and the advantages of each.

5.1 Introduction

Almost any signal processing circuitry requires the establishment of constant bias voltages. Starting with the 60Hz voltage supply from the power company, how do instruments obtain these various DC supply voltages? We will investigate a sequence of circuits for doing this. They all rely on *non-linear elements* that respond differently to different parts of the AC voltage signal.

First, we need to establish some notation (briefly addressed in Lab 2). AC sinusoidal signals are frequently referred to in terms of their *rms* voltages. *rms* stands for "root-mean-square" or, more explicitly, the square-root of the average (or mean) of the squared voltage. Note that if $v(t) = V \cos \omega t$, then the average voltage,

$$\bar{v} = \frac{1}{T} \int_0^T dt\ v(t), \tag{17}$$

is zero, when we take the average over an integer number of periods. The *rms* voltage is

$$V_{rms} = \left[\frac{1}{T} \int_0^T\ dt\ V^2\ \cos^2 \omega t \right]^{1/2} = \frac{V}{\sqrt{2}} \tag{18}$$

since the average value of the $\cos^2(\omega t)$ is 1/2.[1] We reach the conclusion that

$$V_{rms} = \frac{V}{\sqrt{2}} = \frac{V_{pp}}{2\sqrt{2}}. \tag{19}$$

Thus, the "110 Volt" power outlet (where the 110 Volts refers to the rms value) corresponds to $v_{outlet}(t) = \sqrt{2}(110V) \cos \omega t = 155 \cos \omega t$ Volts or 310 Volts peak-to-peak. One justification for using *rms* voltages is that the average power delivered to a resistive load is

$$\bar{P} = \frac{1}{T} \int_0^T\ dt\ \frac{V^2}{R}\ \cos^2 \omega t = \frac{V_{rms}^2}{R}; \tag{20}$$

[1]Recall that $\cos^2 \theta = (1 + \cos 2\theta)/2$ (draw yourself a picture to verify this); the second term has average zero and the constant term clearly has an average of 1/2.

as far as power dissipation is concerned, V_{rms} acts the same as the corresponding DC voltage.

While the oscilloscope displays the details of instantaneous waveforms, typical digital volt meters (DVM) such as the Metex meters read *rms* voltages when set on "AC Volts" scales. *The latter meters are only reliable for sinusoidal signals with frequencies in the vicinity of 60 Hz.*

In this lab, you will use a transformer to generate a roughly 14 Volt (*rms*) AC signal from which you will obtain various approximations to a constant DC voltage. **While the transformer steps down the 110 Volt line voltage, the output can supply large currents! Be sure to wire and check your circuit before plugging the transformer in and be sure that all three output wires from the transformer are plugged into terminal posts on your protoboards.** The secondary side of the transformer is "center tapped"; we will use one side and the center tap — the other wire should just be plugged into a terminal post which is not wired to anything:

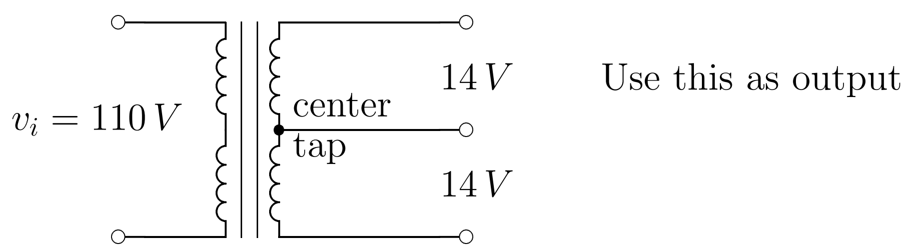

Figure 13: Transformer

One advantage of using a transformer (beyond the obvious reduction in voltage and, thus, danger) is that while the primary voltage oscillates relative to ground potential, the secondary can "float" to any necessary level (within the limits of insulation used inside the transformer). This is a useful feature for the measurements you will make on the "diode bridge" circuits used below. Note that when you measure a voltage signal using the oscilloscope, you are grounding a point in the circuit. You need to think before doing this: you may alter the functioning of the circuit significantly and you could also cause large currents to flow through circuit elements **thus generating a characteristic odor and smoke**! You can measure across floating elements more or less with impunity. The Metex meters, on the other hand, are not grounded so they can be connected anywhere in a circuit regardless whether it is floating or not.

5.2 Procedure

5.2.1 Transformer

Observe, on the oscilloscope, the output waveform of the transformer. Note the frequency and amplitude. Measure this same signal using the Metex meter. Is the Metex reading consistent with the observed waveform? Document what you observe in your lab notebook.

5.2.2 Half wave rectifier.

A simple series connected diode which blocks half the AC waveform leaves you with a finite DC or average level. Use the oscilloscope to observe the output waveform of the circuit shown in Fig. 14. Can you compute the average, or DC, voltage? Is what you see consistent with part (1) and with the diode curves you measured in Lab 1? Use $R_L = 1k\Omega$. Draw a sketch of what you observe in your lab notebook (or capture a sweep and make a plot of the data).

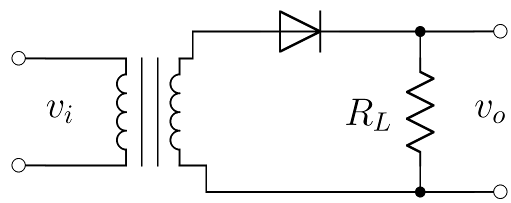

Figure 14: A half-wave rectifier using a 1N4004 diode. The input voltage, v_i, is the AC from the wall outlet.

5.2.3 Full wave rectifier.

The diode "bridge" circuit shown in Fig. 15 directs current always in the same direction through the load. Verify this statement by tracing the current path available when the top transformer terminal is positive (and negative) with respect to the bottom terminal. Construct the circuit (without the capacitor C_f) and observe the waveform. What, roughly, is the DC, or average, voltage? Confirm your expectation by switching the oscilloscope input to the AC coupled setting. How does this signal change when you use a 1kΩ vs a 10kΩ load resistor? Draw a sketch of what you observe in your lab notebook (or capture).

5.2.4 Full wave rectifier with filtering

To smooth the output and better approximate a constant voltage, place a capacitor across the output as shown in Fig. 15. What is the relevant quantity which determines how "constant" the voltage is? Which resistance sets the characteristic time of this low-pass filter? Do you want a small or a large capacitor? Why? Try $C_f = 0.2\mu$F, then a 25μF electrolytic capacitor (be sure to observe the polarity here!). What *resistance* combines with the capacitance to set the characteristic time of this low-pass filter? In each case, measure the ripple voltage (peak-to-peak fluctuation). How does the DC voltage vary with load – i.e., characterize the "voltage regulation"?

5.2.5 Integrated circuit regulator

The simplest way to make a good DC supply for real circuits is to build a rudimentary DC supply such as the one in Sec. 5.2.4 and then use an integrated circuit (IC) "voltage regulator" to stabilize it. Construct the circuit shown in Fig. 16 using an LM7805 which is a

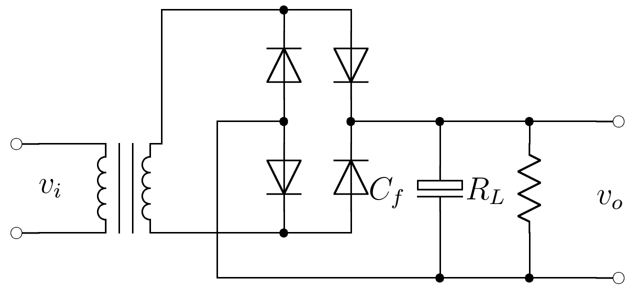

Figure 15: A full-wave rectifier using four 1N4004 diodes, and an electrolitic filtering capacitor. The input voltage, v_i is the AC from the wall outlet.

5 Volt supply regulator (spec sheets attached). The diagram on the first spec sheet looks at the device from the labelled side. We use this IC as a "black box" and just empirically note the quality of performance (the LM7805 costs $1.18). How does the DC voltage vary with load? You probably own several power supplies of this sort in various pieces of electronics.

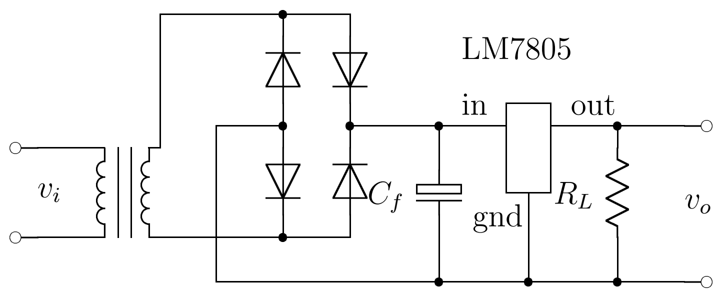

Figure 16: A full-wave rectifier with four 1N4004 diodes, an electrolitic filtering capacitor, and an LM7805 regulator chip. The input voltage, v_i is the AC from the wall outlet.

6 Bipolar Junction Transistors, Emitter Followers

Reference Reading: Chapter 5, Sections 5.1, 5.2 and 5.3.1.
Three lab periods will be devoted to this lab.
Goals:

1. Understand basic transistor operation
2. Understand the need for a biasing network and the design criteria for AC circuits
3. Demonstrate power gain, high input resistance, low output resistance
4. Understand the implication of power gain without voltage gain

6.1 Introduction

Active circuits are ones which can yield "gain" in the sense of being able to yield greater power output than input. In most cases, more power can be delivered to a load by passing the signal through an amplifier than directly from a signal source. Obviously, the gained power has to come from somewhere and this is generally from a DC voltage supply (often called a D.C. power supply for this reason).

We begin with a simple "voltage follower" circuit that provides an output voltage that "follows" the input voltage (i.e., is essentially equal to the input voltage). How can such a seemingly useless circuit have any function? Because it can be a *power amplifier*: because the follower's output impedance (essentially a resistance) can be quite low compared to that of the signal source, the follower can supply more power to a load than a high impedance source could.

In Lab 7, you will examine the common emitter amplifier circuit; this can have both voltage and power gain.

For both labs 6 and 7, we use a simple model for *npn* transistor operation (to understand the underlying principles requires an understanding of how electrons behave in crystals – the subject of a course in solid state physics; in class, we will give a quick introduction):

1. The collector must be more positive than the emitter. This is clearly necessary in order for current to flow from collector to emitter.
2. The base-emitter and base-collector junctions behave like diodes:
   (a) When the base-emitter junction is reverse biased, the transistor is turned off and no current flows from collector to emitter. The base-emitter junction is like the handle of a valve – it controls the current flow through the collector-emitter circuit.
   (b) When the base-emitter is forward biased and the base-collector is reverse biased, the transistor is in the "active" or "linear" operating range. A forward biased diode has a "diode drop" of 0.6 to 0.7 Volts (0.65 V).

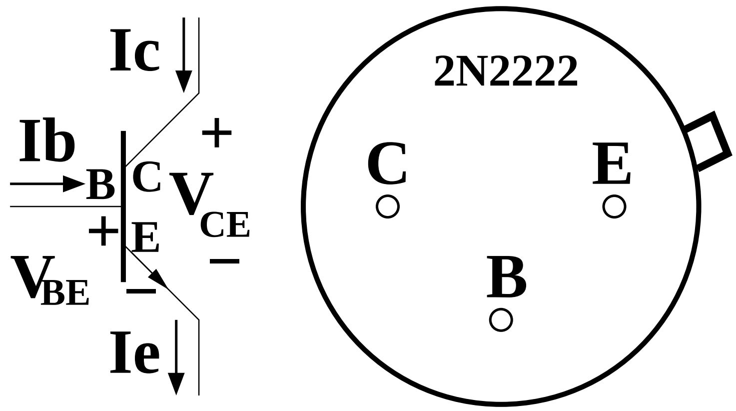

Figure 17: NPN transistor schematic symbol, notation, and lead configuration for the 2N2222.

(c) When both junctions are forward biased, the transistor is "saturated" and, typically, $V_{CE} \approx 0.1 - 0.2$ Volts.

3. Maximum values of I_C and V_{CE} cannot be exceeded without burning out the transistor.

4. If 1 - 3 are obeyed, then $I_C \approx h_{FE} I_B = \beta I_B$. β (or h_{FE}) is roughly constant in the active or linear operating range. Typical values are in the range 50 - 250 and can vary substantially from transistor-to-transistor even for a given transistor type. A good circuit design is one that does not depend critically on the exact value of β but only on the fact that β is a large number.

Figure 17 illustrates the definitions of transistor voltages and currents. Note that it is always true that

$$I_E = I_C + I_B \,. \tag{21}$$

In the active range,

$$I_E = (\beta + 1) I_B \approx I_C, \tag{22}$$

the approximation holding for large β, and

$$V_B \approx V_E + 0.65\text{Volts}. \tag{23}$$

You will apply these equations many times – remember them!

Also shown is a picture of the 2N2222 transistor as seen from the side with the leads. You should remember that the metal transistor can is usually connected to the collector – *be careful to not let wires touch the can!*

You can verify that a transistor is functional by checking the two diode junctions with an ohmmeter. With the positive (red) lead on the base of an NPN transistor, you should see conduction to both emitter and collector; with the negative (black) lead on the base, you should not see conduction to either other lead.

For the emitter follower, we will (in class) determine the input resistance to be

$$R_i = (\beta + 1)R_e, \tag{24}$$

where R_e is the equivalent resistance from the emitter terminal to ground. For the output resistance we will obtain,

$$R_o = \frac{R_s}{\beta + 1}, \tag{25}$$

where R_s is the equivalent source resistance. Hence, a large β helps make the input resistance high (the circuit draws only a small amount of current and therefore receives the maximum voltage signal from the source) and the output resistance low (the output voltage is independent of the load–i.e., of the current drawn–down to small loads). *When you see such statements as these, you should think of (and even draw) Thèvenin equivalent circuits; here, draw (i) the equivalent circuit of a source and the input of the transistor circuit and (ii) the equivalent for the transistor circuit output and a load – justify the statements.*

6.2 Procedure

First, you will demonstrate the *impedance transformer* property of the emitter follower using just DC voltages. To take advantage of this same property, but applied to AC signals, requires some additional complications that you will learn about in 6.2.2.

6.2.1 DC Emitter Follower

Use an emitter follower circuit to make a good voltage source out of a lousy one. You should recall from previous work what constitutes a "good" voltage source. The circuit in Figure 18 shows a voltage divider driving an emitter follower circuit. The large resistances ($4.7\,k\Omega$) in the divider mean that any load driven by the divider would need to have a resistance much larger than $4.7\,k\Omega$, making this "lousy voltage source".

We are going to combine this with the transistor "emitter follower" to make a voltage source whose output terminals are indicated by the two open dots near V_0 in Figure 18. You should think of everything up to those dots as being the new and improved "voltage source" whose characteristics you want to measure.

1. First, in your notebook, draw the circuit with the input (the voltage divider) replaced by its Thèvenin equivalent. Draw the transistor circuit attached to this equivalent. Next, draw the same equivalent circuit of the voltage divider with the transistor circuit replaced by its equivalent as seen from the base; what is the value of the load resistance seen by the voltage divider?

2. On the same graph you will use for the emitter follower output, draw the *expected* I-V curve for the divider circuit; i.e., for the Thèvenin equivalent just drawn. Use axes that show the global behavior, going from zero to the maximum values of I and V.

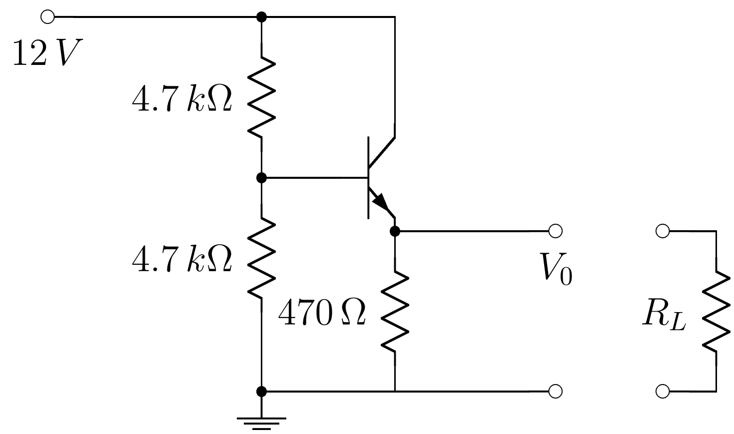

Figure 18: DC Emitter Follower Circuit. This circuit is an impedance transformer in that the I-V characteristic of the output terminals (∘) has a slope that corresponds to a smaller source resistance than does the I-V characteristic of the "Voltage Divider Source" by itself. Because the circuit delivers more power to a small load, R_L, than the "Voltage Divider Source" would by itself, the emitter follower can have significant power gain.

3. Build the circuit shown in Fig. 18. You can use the on-board 12V power supply as the DC source. *With multi-part circuits, it is always a good idea to build and test the circuit in sections. Follow this sequence:*

   (a) Build the voltage divider first. Test the output voltage and verify that it is as expected. You might want to put a load resistor across the output to make sure your work above is correct.

   (b) Add the transistor and emitter resistor but keep $R_L = \infty$. It is advisable to ground the negative side of the DC power supply used to supply 12V to the divider and the transistor. Note that because the DC supply is such a good voltage source (constant voltage regardless of current being supplied), you can think of it as independently supplying 12V to both parts of the circuit.

   (c) What is the voltage divider output now? Is this as expected?

   (d) Is V_0 the expected value?

   (e) If your measurements for any of the above are puzzling, check the DC supply voltage – is this being shorted out? Is the power turned on?

4. Measure and plot, on the same axes as above, the I-V curve for the emitter follower output (do this by varying the load on your circuit in a way similar to that used in Lab 1). From this plot, determine the equivalent output resistance, R_o, of the circuit and compare to equation 25.

5. Determine the answers to the following questions:

(a) What is the power delivered to a load in the two cases (with and without the emitter follower) when $R_L = 500\Omega$?

(b) How sensitive is this circuit to the precise value of β?

(c) What would happen to the functioning of this circuit if we chose voltage divider resistors of $100k\Omega$ (perhaps to reduce power consumption)?

(d) What are the minimum and maximum input voltages this circuit can "follow" (given a fixed 12V supply at the collector)?

6.2.2 AC Emitter Follower

Before going further, you should understand how the circuit in Fig. 19 operates. What are the functions of C_1 and C_2? What do R_1 and R_2 achieve? Once you understand the design principles of this circuit, follow the steps below to select appropriate components for an audio amplifier.

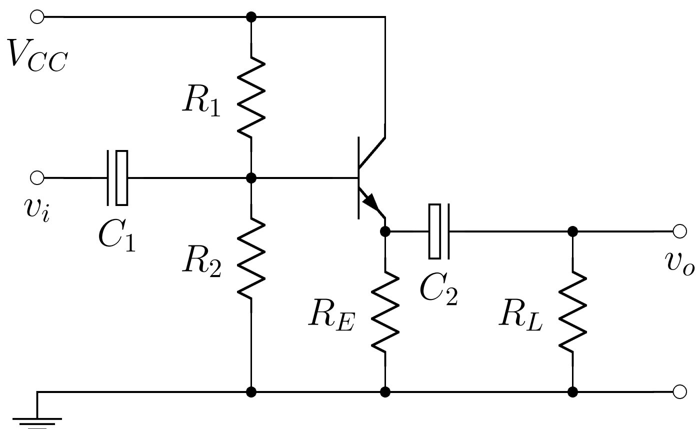

Figure 19: The AC emitter follower circuit.

- Follow the design procedure in the example at the end of section 5.3.1 of the textbook to determine appropriate values of components for the audio amplifier circuit. Here, we are using the same $V_{CC} = 12$ Volts but use $I_C = 10\,mA$ instead of $1\,mA$. Be sure to record your calculations in your lab notebook.

- Test the functioning of your circuit at, say, $1\,kHz$ to see how large an input voltage you can use with a large load resistor (say, $R_L = 10\,k\Omega$).

- Measure the frequency response from just below your designed cut-off frequency up to the highest possible frequencies. Do this using an input amplitude which is somewhat smaller than the maximum possible (say $5\,V$ amplitude). Compare the results with $R_L = 1\,k\Omega$ and $R_L = 100\Omega$ (just check a few relevant frequencies for these last tests, so you can map out the response in the region in which it is changing).

- From your frequency response, predict how this circuit would respond to triangle or square wave inputs. Try it for some appropriate period of the input wave (using a value of R_L for which the circuit works well), and see if you are right. Try 5 or 10 kHz waves, if the expected distortion isn't clearly visible, try higher or lower frequencies. Include a sketch of the resulting waveforms (or capture and plot it) and appropriate discussions in your lab notebook.

- Test a design using different quiescent current, I_C. Try $1mA$ and make minimal changes in the circuit (do R_1 and R_2 need to be changed? explain). Test the circuit operation: can large AC signals still be passed? Does the low-frequency cut-off change? Is the high-frequency behavior still the same?

7 Bipolar Junction Transistor: Inverting Amplifiers

Reference Reading: Chapter 5, Sections 5.3.2 and 5.3.3.
Three lab periods will be devoted to this lab.
Goals:

1. Learn to set up a common emitter voltage amplifier

2. Learn the limits: relatively low input resistance, relatively high output resistance, frequency response.

3. Learn AC biasing tricks to get higher gain.

7.1 Introduction

The common emitter amplifier appears to be a subtle variation on the emitter follower studied in lab 6. The collector is attached to the supply through a resistor instead of directly and the output is taken from the collector terminal of the transistor instead of the emitter. The emitter may be connected directly to the ground. (Hence the name, *common emitter*, since the input and output signals share the common ground at the emitter.) As discussed in the text, this gives a large gain but has poor linearity, an input impedance that is a function of input voltage, and is difficult to bias properly. We will use the slightly modified inverting amplifier that includes a resistor R_E between the emitter and ground as shown in Fig. 20. We will find that the gain of the amplifier can be controlled with proper selection of R_E.

In spite of the similarities, the behavior of this circuit is significantly different from the emitter follower:

1. We can arrange for significant voltage gain.

2. The output signal (that is, the AC signal) is inverted relative to the input.

3. The output resistance is quite a lot larger than that of the emitter follower.

The gain, G is computed as follows:

1. The emitter voltage "follows" as before: $V_E = V_B - 0.65\text{V}$. Thus, $v_E = v_B$.

2. v_E generates an AC current $i_E = v_E/R_E = v_B/R_E$.

3. Using $i_E \approx i_C$, this AC current generates an output voltage $v_C = -i_E R_C = -v_B \frac{R_C}{R_E}$. Thus,
$$G = -\frac{R_C}{R_E}. \tag{26}$$
The minus sign indicates that when V_B increases, V_C decreases. This makes sense since $V_C = V_{CC} - I_C R_C$ and I_C increases when V_B increases.

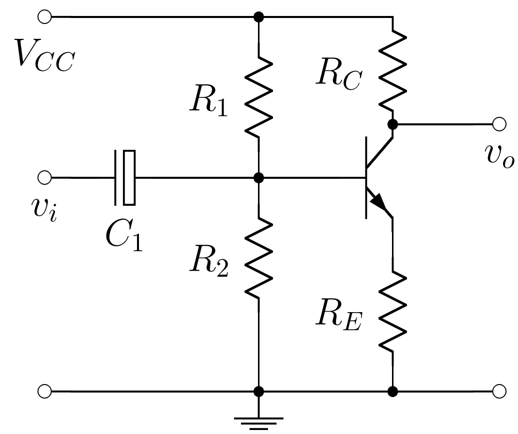

Figure 20: Inverting amplifier

If we try to decrease R_E toward zero to get higher gain, we find that the intrinsic emitter resistance, r_E becomes important and limits the gain. r_E accounts for the fact that our standard "diode drop" of 0.65 Volts is only an approximation. The drop, V_{BE}, is actually a function of the current through the diode junction as you saw in Lab 1. Based on the I-V characteristic of a diode, the text argues that $r_E \approx \frac{25\Omega \cdot mA}{I_C}$ near room temperature. For $I_C = 10\,mA$, $r_E =\approx 2.5\Omega$ (this means that for a 1mA change in current, V_{BE} changes by $2.5\,mV$ out of the roughly 0.65 Volt total drop). We should write

$$G = -\frac{R_C}{R_E + r_E}\,. \tag{27}$$

In deciding on component values, we need to change the base bias resistor values (relative to the emitter follower) in order to set the collector operating point (the collector voltage at zero AC input) near $V_{CC}/2$; again, we do this so as to maximize the possible output voltage swing (which certainly cannot extend below zero volts or above V_{CC}). Recall that for the follower, we biased so that the *emitter voltage* (which was then the output) satisfied this requirement. Now we require that

$$V_C = V_{CC} - I_C R_C \approx \frac{1}{2} V_{CC} \tag{28}$$

or

$$I_C = \frac{1}{2}\,\frac{V_{CC}}{R_C} \approx I_E = \frac{V_E}{R_E} = \frac{|G|}{R_C} V_E\,. \tag{29}$$

This means that we want

$$V_E = \frac{1}{2}\,\frac{V_{CC}}{|G|}. \tag{30}$$

And now we know that

$$V_B = V_E + 0.65\text{Volts} = \frac{1}{2}\,\frac{V_{CC}}{|G|} + 0.65\text{Volts}. \tag{31}$$

This is a lower base voltage than we used for the follower which means that the base or input voltage won't be able to swing as far as in the follower case (without turning off the transistor). This is okay: we are building a voltage amplifier because we only have a small signal to begin with!

The output resistance of this circuit (i.e., the Thevenin equivalent resistance at the output) is just R_C. You should always remember that the collector behaves like a current source and has large resistance (the I_C-V_{CE} characteristic curves are nearly horizontal; the current of the current source is controlled by the base-emitter voltage – see section 5.3.3). To get high gain, we want large R_C, but we pay by having a large output impedance.

In selecting R_1 and R_2, keep in mind that we want the base bias voltage to be fairly independent of the β of the transistor. To do this, we want the base bias circuit to yield the same voltage when attached to the transistor as it does all by itself. In other words (#1), we want to lose only a small fraction of the divider's current into the base. In other words (#2), the Thevenin equivalent resistance of the bias circuit should be small compared to the input resistance of the base (this is the same logic we used for the follower). The base input resistance is as for the follower:

$$R_{in} \ = \ (\beta + 1) \cdot (R_E + r_E) \ .$$

7.2 Procedure

7.2.1 Inverting Amplifier

Build a common emitter amplifier with a gain of $G = -10$ and an output resistance of $R_C = 4.7\text{k}\Omega$. Use a base bias circuit with an equivalent resistance about 50 times smaller than the input resistance seen at the base. Use $V_{CC} = 12\text{V}$. As indicated below, build the circuit in a modular sequence and check each part before attaching additional pieces.

1. Measure the output voltage of your biasing voltage divider without the transistor attached. After attaching to the transistor circuit, check the change in this voltage.

2. Check V_C. Is it what you planned (or within the expected range)?

3. Choose an input coupling capacitor large enough to generate a roll-off frequency of $\leq$ 20 Hz. *What is the relevant resistance that determines this roll-off? Draw the relevant equivalent circuit and indicate element values.*

4. For a $0.1\,V$ peak-to-peak input at a moderate frequency, sketch (or capture) the voltages V_B,V_E, and V_C.

5. For a $0.1\,V$ peak-to-peak input, measure the frequency dependence of the gain and plot on a Bode plot. Determine the -3dB points (provided you have the frequency range available). *Do you think the high frequency roll-off is due to the scope input impedance or is it intrinsic to the transistor circuit (this could include the possibility of stray capacitance in the circuit)? Draw the equivalent circuit for this measurement.*

6. Pick a mid-range frequency and determine the input voltage dependence of the gain (i.e., *is G dependent on* $|V_{in}|$*?*). *What is the maximum input voltage that yields an undistorted output signal? What is it that limits the output?* It may help here to view the output alternately using DC and AC coupling on the scope: AC to accurately see the signal amplitude, DC to see the actual collector voltage relative to ground and the supply voltage.

7. Measure the output resistance of this circuit. Use a mid-range frequency and a mid-range amplitude. To do this, you need to measure two points on an $I-V$ curve for the output of the transistor. However, we are going to do this using an AC voltage.*Sketch the Thevenin equivalent as seen at the output of the circuit.* To get a second point on the $I-V$ curve, we want to attach a $4.7\,k\Omega$ resistor from the output of the circuit to ground, and then measure the voltage across this **known** resistor. *If we just attached this resistor, what will happen to the DC voltage,* V_C*?* To avoid changing the gain and DC operating point of the circuit, we need to use a blocking capacitor between the output of the circuit and the resistor to ground. This is like what you did for the AC emitter follower. Chooses a sufficiently large capacitor such that it's impedance is small compared to 4.7kΩ at the frequency you are using. *Do you see the expected result?*

7.2.2 Inverting Amplifier With By-Pass Capacitor

Now try boosting the gain by placing a "by-pass" capacitor across R_E as shown in Fig. 21 (see discussion of Fig. 5.29 in the textbook). As in the previous measurment, this capacitor will not affect the DC operation of the circuit. However, at signal frequencies, the capacitor should effectively *short out* the emitter resistor R_E and the gain becomes $G = -\frac{R_C}{r_e}$. Measure the frequency response and the range of input linearity for this circuit and compare to the lower gain circuit studied above. Make sure that you try to measure both the low-frequency and the high-frequency $3\,dB$ points.

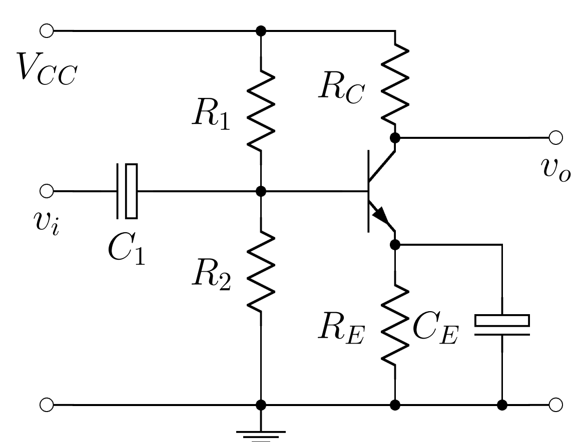

Figure 21: Inverting amplifier with bypass capacitor

There are several points you need to be aware of before trying this circuit. Read through all four of these points and understand them before starting to the measurements in this section.

1. You have to be careful in determining what C_E you need to achieve the desired time constant. The emitter by-pass capacitor sees R_E in parallel with [r_e in series with the input and biasing circuits]. At signal frequencies, this amounts to $[r_e + R_s/\beta] \approx r_e$, R_s being the signal source resistance which is 50Ω in our case. Recall that $\mathrm{r_e} \approx 25/\mathrm{I_C}(\mathrm{mA})$. You will find that you need quite a large capacitor for the circuit to operate down to 20Hz.

2. The gain may be quite high. If $G \approx -200$, then a 0.1V input (the minimum the DS335 will generate) would generate a 20V output. With a 12 Volt supply, this won't work. You will need to attenuate the input signal by building an input voltage divider. Put the output of the DS335 into our divider and use the ouptut of this new divider to drive your circuit. To build the divider, use 100Ω resistor in series with 10Ω resitor in order to maintain a low source resistance.

3. When you have such a small input signal, you may find that the input signal is extremely noisy. If you study this carefully, you are likely to find that it is a 60 Hz signal that is coming in through your 12 V DC power supply. If this is a case, use the large DC supply that was used in lab 1 to provide the DC voltage. You will find that this is probably significantly less noisy.

4. Be sure to observe the proper polarity for the required electrolytic capacitor.

Note: you can have better control of the AC gain by using the circuit shown in Figure 22. The bypass resistor, R_b is some fraction of R_E. In this configuration, only some of the emitter resistance is by-passed.

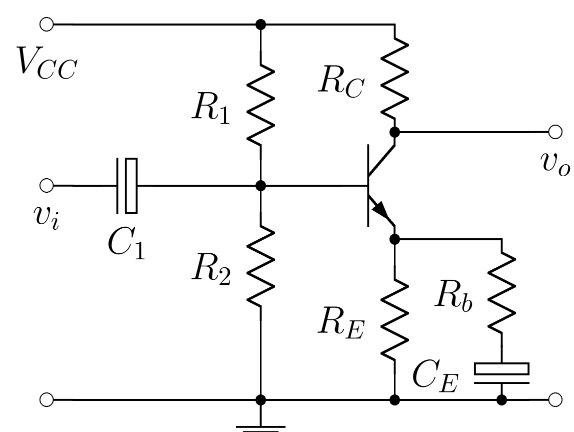

Figure 22: Inverting amplifier with a bypass capacitor an resistor.

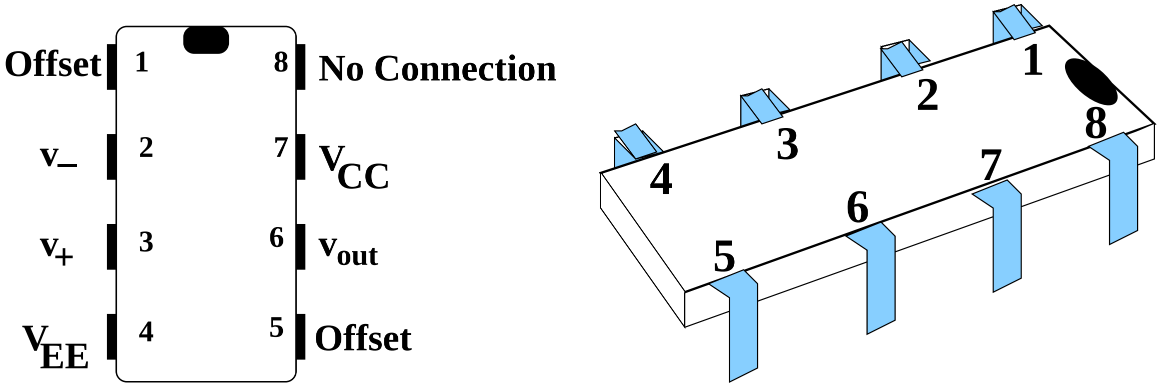

Figure 23: 741 and 411 op-amp pin connections

8 Introduction to Operational Amplifiers

Reference Reading: Chapter 6, Sections 6.1, 6.2, 6.3 and 6.4.
Two and one half lab periods will be devoted to this lab.
Goals:

1. Understand the use of negative feedback to control amplification
2. Understand the concept of *slew rate*
   (a) Be able to define slew rate
   (b) Be able to measure slew rate
   (c) Understand how finite slew rate puts limitations on the use of operational amplifiers
3. Be able to design and construct the following op-amp circuits:
   (a) Voltage follower
   (b) Inverting amplifier
4. Observe the effect of an op-amp's finite gain

8.1 Introduction

Read text sections 6.1 through 6.4 of your textbook before starting.

For reference, the pin configuration for the 741 and the 411 op-amps is shown below. You will use the Proto-board power supply to power the op-amp. You should print out (in advance) the specification sheets for the op-amps, which are available on the "Labs" web page. You may want to compare your results to the specifications.

8.2 Procedure

8.2.1 Voltage Follower

Use a 741 op amp to build a voltage follower as in Fig. 24. Note that, as is conventional, the power pin connections, $+V_{CC}$ and $-V_{EE}$, are not indicated on the diagram (but you need to include them) and we use no connection to the offset null pins.

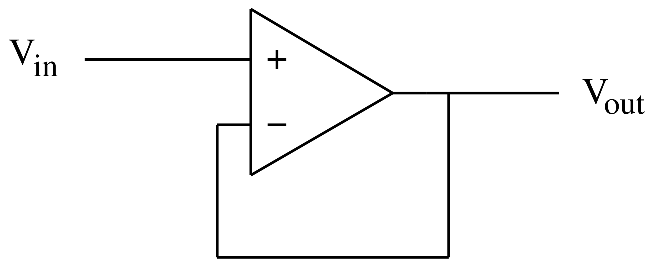

Figure 24: Voltage follower circuit

1. **Slew Rate.** Start by investigating one of the serious limitations of many op-amps: the slew rate. The slew rate is the maximum rate at which the output voltage can change. (Typical units would be volts per microsecond.) The effect of an op-amp's slew rate limitation is illustrated for two output waveforms in Fig. 25.

   - Measure the slew rate of the 741 by using a square wave input and observing the output of the follower. At an input amplitude of, say, $V_{pp} = 5$ V, the output square wave will not change abruptly, but will change to the new value by a straight line with finite slope. The slope of the line gives the slew rate. You will have to adjust the DS335 square wave period (and scope time scale) to find where you can observe this phenomenon.
   - To understand the connection between slew rate and frequency response, calculate the maximum rate of change of a sinusoidal voltage, $v(t) = V \cos \omega t$. Use this result to find the relation between amplitude and frequency for which this maximum rate of change equals the 741's slew rate. What is the maximum frequency (in Hz) you can use without encountering slew rate distortion if the signal is 5 Volts peak-to-peak? 1 Volt? 0.1 Volt?
   - Make the same measurements for the 411 op-amp and compare to the 741.

2. **Gain.** It is difficult to measure the open loop gain of even the 741 op-amp because it is so large. However, at high frequencies, the gain rolls off and becomes measurable.

   (a) Compare the input and output voltages a follower built using the **741 op-amp** over the **entire** frequency range of the DS335. Use an input of $V_{pp} = 0.1$ V (why?). Make a Bode plot of the gain, $|G(f)|$, and a plot of the phase shift, $\phi(f)$, between input and output signals.

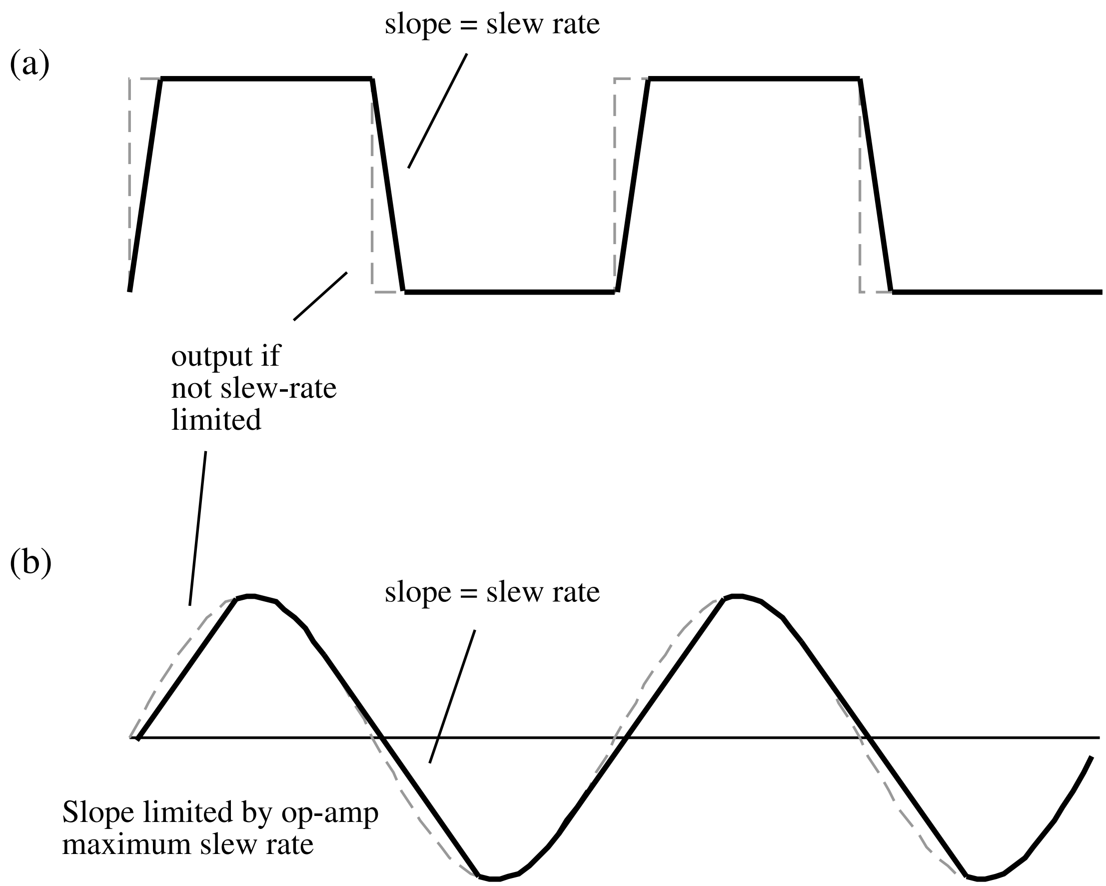

Figure 25: Slew rate limitations illustrated for square wave and sinusoidal wave inputs.

(b) Observe the effect of larger input voltages. You should see distortion in the output at high frequencies when the input signal exceeds the slew rate.

(c) Repeat the previous measurements using the **411 op-amp**.

From the above small-signal measurements, you can determine the high-frequency open-loop gain, $\mathbf{A}(f)$ of the 741 (i.e., the differential gain), but some analysis is required. The output voltage is

$$\mathbf{V}_o = \mathbf{A}(f)(\mathbf{V}_+ - \mathbf{V}_-). \tag{32}$$

The relation between the op-amp's open loop gain $\mathbf{A}(f)$ and the actual gain of the circuit $\mathbf{G}(f)$ depends on the negative feedback loop in the circuit. In a *voltage follower* circuit, input is connected to $\mathbf{V}_+$ and the output is connected directly to $\mathbf{V}_-$. Thus $\mathbf{V}_o = \mathbf{A}(\mathbf{V}_{in} - \mathbf{V}_o)$ or

$$\mathbf{G}(f) \equiv \frac{\mathbf{V}_o}{\mathbf{V}_{in}} = \frac{\mathbf{A}}{\mathbf{A}+1}. \tag{33}$$

This equation can be inverted to give

$$\mathbf{A}(f) = \frac{\mathbf{G}(f)}{1 - \mathbf{G}(f)} \tag{34}$$

Keep in mind that all bold faced quantities are complex numbers. To determine $|\mathbf{A}(f)|$, you can write $\mathbf{G}(f) = G(f)e^{j\phi(f)}$ to obtain

$$A(f) = \frac{G}{[1 + G^2 - 2G\cos\phi]^{1/2}}. \tag{35}$$

For both the 741 and the 411 op-amps, make a Bode plot of $A(f)$ in the region where you can measure it (from (34) or (35), when $G \approx 1$ and $\phi \approx 0$, A is large and difficult to measure quantitatively) and determine the slope of the straight line that best fits the high frequency region of the results. Find the frequency, f_T at which the magnitude of the open loop gain $A(f)$ is unity.

3. **Follower Input and Output Impedances.** It is also difficult to measure either the input or output impedances of this circuit. Use the **411 op-amp** for the following:

   (a) To show that the output impedance is small, observe the gain at 1 kHz with an output load of 10 Ω. Note that the maximum output current of the 411 is about 20 mA, so limit the output voltage to less than 200 mVolts. Can you calculate the output impedance from this measurement? Is it large or small?

   (b) To demonstrate the large input impedance, insert an 8.2 MΩ resistance in series with the input and compare the gain at 1 kHz to that measured with a direct input from the DS335. What does this say about the input impedance of the follower?

8.2.2 The Inverting Amplifier

Here, you will construct and test two inverting amplifier circuits, one with gain, $G = -10$ and one with $G = -100$. The tests include determination of the DC gain (for the $G = -10$ case only) and a comparison of the frequency responses of the two circuits (these will also be compared to that of the voltage follower measured previously). You will use a fixed input resistance of 1 kΩ and the only the **741 op-amp**.

The zeroth-order analysis of the circuit shown in Fig. 26 goes as follows:

1. The op-amp gain is infinite, its input resistance is infinite. Then, the feedback resistance must keep the inverting input at ground. Thus, $i_{in} = v_{in}/R_{in} = i_f = -v_o/R_f$. The minus sign indicates that v_o must be below ground for positive v_{in} in order for the current to flow from ground (v_-) to v_o.

2. The above equations can be solved for $G = \frac{v_o}{v_{in}} = -\frac{R_f}{R_{in}}$.

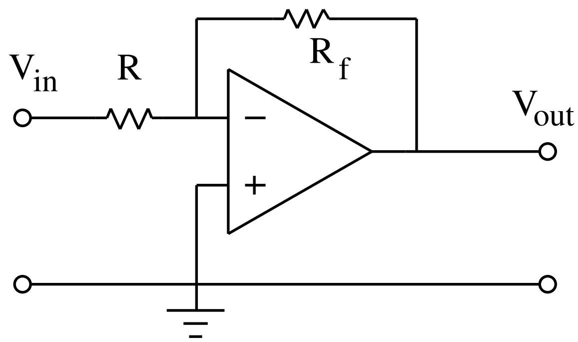

Figure 26: Inverting Voltage Amplifier

3. Of course, you want to use an input resistor which is larger than your source resistance.
4. Within the limitations of the op-amp to supply current and voltage, the output resistance is very low as before.

1. **Design and build the $G = -10$ amplifier.**
   (a) Measure the DC output voltage as you vary a DC input voltage. Vary the input so as to make the output cover the full range of ±12V. The slope of this plot yields the DC gain. Does your plot pass through the origin? Does the output reach the supply voltages?
   (b) Measure and make a Bode plot of the frequency response of your amplifier (you need only measure the amplitude response, not the phase shift). Keep in mind (and avoid) the slew rate limitation of the 741 op amp. Plot $20 \log G(\omega)$ on scales which will allow you to add the $G = -100$ measurements you will do next.
2. **Build the $G = -100$ amplifier**
   (a) Measure the frequency (amplitude) response of your amplifier. Add these data to the plot you began above.

To understand what you see in the above measurements, we again have to go beyond the zeroth order analysis. Here's how that goes: We admit that the op-amp gain is not infinite (we already know it is reduced at high frequencies) but we keep the approximation that the input resistance is high.

1. Since $\mathbf{V}_+ \equiv \mathbf{0}$, $\mathbf{V}_o = -\mathbf{A}(\omega)\mathbf{V}_-$ or $\mathbf{V}_- = -\frac{\mathbf{V}_o}{\mathbf{A}}$. Here, $\mathbf{A}$ is the complex open-loop differential gain of the op-amp.
2. $\mathbf{I}_{in} = (\mathbf{V}_{in} - \mathbf{V}_-)/R_{in} = \mathbf{I}_f = -(\mathbf{V}_o - \mathbf{V}_-)/R_f$. (Still taking the input impedance to be ≈ infinite.)
3. Substituting for $\mathbf{V}_-$ and collecting the $\mathbf{V}_o$ terms, we have $\mathbf{V}_{in} = -\mathbf{V}_o(\frac{R_{in}}{R_f} + \frac{1}{\mathbf{A}} + \frac{R_{in}}{\mathbf{A}R_f})$.

4. Calling $R_f/R_{in} \equiv G_\infty$ (the absolute value of the gain if the op-amp gain is infinite), we can re-arrange this to

$$\mathbf{G}(\omega) = -G_\infty \left(\frac{\mathbf{A}}{\mathbf{A} + G_\infty + 1} \right). \tag{36}$$

5. As long as $|A| >> |G_\infty|$, $\mathbf{G} = -G_\infty$ as we got from the simple calculation.

6. As $|A|$ becomes less than $|G_\infty|$, $\mathbf{G} = \frac{\mathbf{A}}{1+1/G_\infty} \approx \mathbf{A}$, which is almost independent of the intended G_∞ when this number is large (this is the result you should observe at high frequency). What you have measured is $|G(\omega)|$ which should become equal to $|A(\omega)|$ at high frequency. You should see that each circuit becomes limited by $\mathbf{A}$ at a different frequency. What is the product of $|G_\infty|$ and the -3 dB frequency in each case (this is called the gain-bandwidth product)?

7. A very useful plot to make and discuss in your lab report is one that contains the Bode plots for the $\times 10$ and $\times 100$ circuits as well as the open-loop gain of the op-amp: (**hint:** do this).

9 Operational Amplifiers with Reactive Elements

Reference Reading: Chapter 6, Sections 6.5 and 6.6.
Two and one haalf lab periods will be devoted to this lab.
Goals:

1. Be able to design and construct the following op-amp circuits:
   (a) Integrator
   (b) Differentiator
   (c) Logarithmic amplifier

9.1 Introduction

All the circuits here are based on the inverting amplifier configuration of the last lab. However, we find here that we can make circuits that perform mathematical functions (integrators and differentiators) that are far superior to the passive circuits built in lab 4. To obtain the best functionality, we use the 411 op-amp.

9.1.1 The Integrator

We will first consider the simple integrating circuit shown in Fig. 27a. For this circuit, the inverting input, v_-, is a virtual ground because the op-amp golden rules tell us v_-=v_+. The second golden rule (no current into the inputs) tells us that the current through R_{in} also goes through C_f. Thus $i = dQ_C/dt = v_{in}/R_{in}$. Since $Q = -C_f\ v_o$, we get

$$-C_f \frac{dv_o}{dt} = \frac{v_{in}}{R_{in}} \tag{37}$$

or

$$v_o(t) = -\frac{1}{R_{in}C_f}\int_0^t v_{in} dt \tag{38}$$

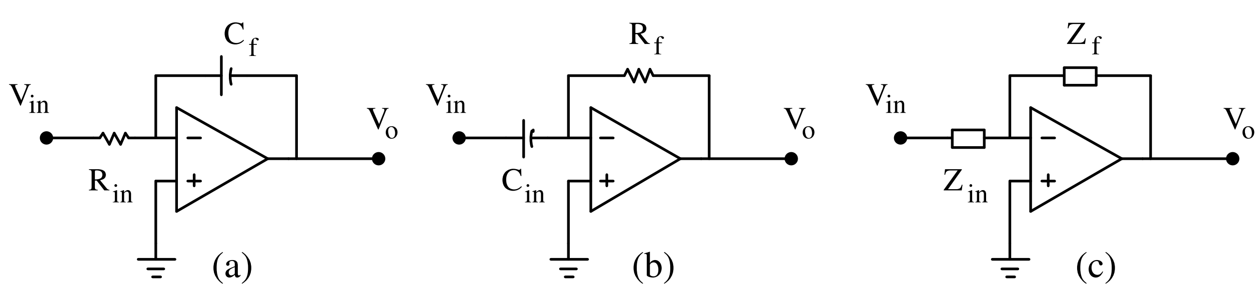

Figure 27: Idealized circuits for a) integrator, b) differentiator, and c) generalized inverting amplifier.

This *time domain* treatment shows that the output is $1/(R_{in}C_f)$ times the integral of the input voltage. It is also instructive to consider the behavior in the *frequency domain*. First note that a time-dependent signal can be written as the sum of sinusoidal signals

$$v(t) = Re\left(\sum_N \mathbf{V_N} e^{j\omega_N t}\right). \tag{39}$$

The integral of the signal has the form

$$\int v(t)dt = Re\left(\sum_N (j\omega_N)^{-1}\ \mathbf{V_N} e^{j\omega_N t}\right). \tag{40}$$

Thus, to form the integral of a general waveform, we need a magnitude response that scales as $1/\omega$ and that has a 90° phase shift over the relevant frequency range. Since the gain of the generalized inverting amplifier (shown in Fig. 27c) is

$$G = -Z_f/Z_{in}, \tag{41}$$

the gain of the circuit shown in Fig. 27a is just $-(j\omega \mathrm{R_{in}C_f})^{-1}$, so we see that each term is weighted by the $(j\omega_N)^{-1}$ factor required in (40) to give the Fourier components of the integral. This again shows that the output is proportional to the integral of the input with the same $-1/(R_{in}C_f)$ proportionality factor as above.

9.1.2 The Differentiator

The gain of the circuit shown in Fig. 27b is

$$G(\omega) = -Z_f/Z_{in} = -j\omega R_f C_{in} \tag{42}$$

Using (39),

$$\frac{dv}{dt} = Re\left(\sum_N (j\omega_N)\ \mathbf{V_N} e^{j\omega_N t}\right), \tag{43}$$

so to take the derivative, we need to multiply each Fourier coefficient by its frequency, ω, and introduce a 90° phase shift. The factor of $j\omega$ in (42) shows that the circuit does exactly that.

Thus the circuit in Fig. 27b is a *differentiator*. You may wish to prove to yourself (or see your class notes) that a time-domain treatment of the circuit gives the same results.

Complications. In practice, both these idealized circuits suffer from a similar problem. For the integrator, we must realize that the input signal is likely to have a small DC offset. Even a very small DC current will charge up the capacitor and cause the op-amp to reach its maximum output voltage within a short time period. For a *frequency domain* treatment of this problem, remember the gain of the integrator is $(j\omega RC)^{-1}$. Thus any non-zero DC input (which corresponds to $\omega = 0$) will have infinite gain for an idealized op-amp. In reality, this means the op-amp output will reach its maximum voltage very quickly. A practical op-amp integrator circuit must be modified to keep the gain finite at low frequencies.

Similarly, the idealized differentiator has a gain of $j\omega RC$ that becomes large at high frequencies. This is both very difficult to achieve and makes the circuit subject to high frequency noise. A practical circuit will cut off the divergence of the gain at large ω so that the output is not dominated by high frequency noise. The op-amp open-loop gain, $\mathbf{A}(\omega)$, will eventually *reduce* the gain at high frequencies. This implies that there is a peak in the gain somewhat like that in a resonant circuit.

The circuits you build in the following sections will demonstrate, at least to some extent, how to cope with these problems.

9.2 Procedures

9.2.1 Integrator

As discussed above, in the frequency domain, integration amounts to division by $j\omega$. We do not want to integrate any constant or DC part of the input signal (or any output offset in the op-amp), so we set a maximum gain or "cut-off" to the $(j\omega)^{-1}$ dependence. This is done by introducing the resistor R_f in parallel with the feedback capacitor C_f as shown in Fig. 28. For $\omega R_f C_f \gg 1$ the feedback impedance is $(j\omega C_f)^{-1}$ so the circuit behaves as an integrator. For $\omega R_f C_f \ll 1$ the feedback impedance goes to R_f, so the gain approaches R_f/R_i instead of diverging.

- *Choose* R_f. Use an input resistance $\mathrm{R_{in}} = 1\mathrm{k}\Omega$. (Smaller values would reduce the input impedance and larger values would make the following steps more difficult.)

  Once R_{in} is fixed, the DC gain is determined by the value of R_f. If the gain is to decrease with increasing frequency, it is best to have large factor multiplying the $(j\omega)^{-1}$ – i.e., the low frequency gain should be large. Pick R_f so that the DC gain is 100.

- *Choose* C_f. Suppose you want to integrate an input signal whose fundamental frequency is 50 Hz or greater. Choose an appropriate value of C_f so that the circuit will act like an integrator down to about 50 Hz. Compute and sketch the expected form of the frequency response (magnitude) curve, $|G(\omega)|$ (at this point, you shouldn't have to do a complete calculation to sketch this curve!).

- Build the circuit.

- Verify that the frequency response of the circuit goes as $1/f$ in the appropriate frequency range. Note that you can also think of this as a low pass filter – but one with gain, in contrast to the passive RC circuit studied earlier.

- Use a square wave input with a fundamental frequency above the -3 dB point and show that the output resembles the integral. Try other available waveforms. What happens when the input signal frequency becomes too low?

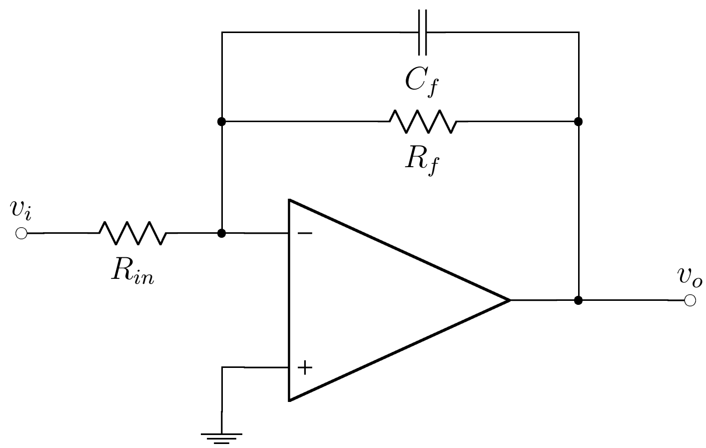

Figure 28: Practical integrator circuit including feedback resistor R_f to introduce a low frequency cutoff.

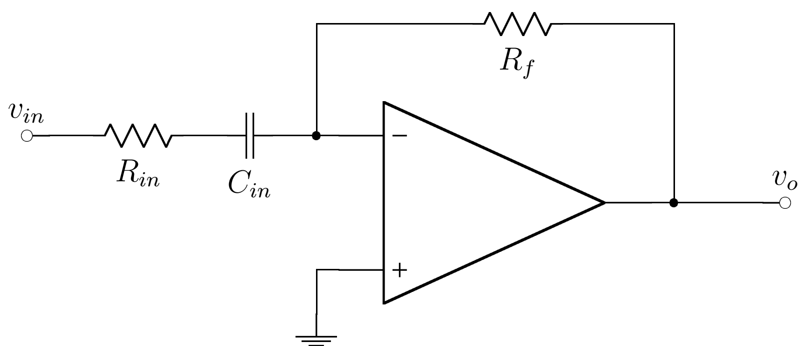

Figure 29: Practical differentiator circuit including input resistor R_{in} to introduce high frequency cutoff.

9.2.2 Differentiator

Differentiation corresponds, in the frequency domain, to multiplication by $j\omega$. Now we have increasing gain as the frequency increases. As you have seen before, the increasing gain will be cut off by the op-amp gain at some point. It is best to have the cut-off determined by external elements instead. High gain at high frequency may also cause slew rate problems for this circuit. By introducing the input resistor R_{in} (Fig. 29), the gain at high frequencies is reduced to $\mathrm{R_f/R_{in}}$.

1. *Choose* R_{in}*,*C_{in}*, and* R_f*.* In this case, referring to the circuit in Fig. 29, we want to set the high frequency gain to be high. Set this gain to be 100 and the minimum input impedance to be 1 kΩ. Set the upper frequency for differentiation to be 5 kHz (this is also the -3 dB point of the high pass filter). Again, compute and sketch the expected shape of the frequency response.

2. Build the circuit shown in Fig. 29.

3. Measure the frequency response (magnitude only), over the relevant frequency range. Does the circuit work as designed? Discuss reasons for any deviations from your expectations.

4. Differentiate both a square wave and a triangle wave. For the triangle wave, quantitatively compare with the expected amplitudes of the derivative. Vary the fundamental frequency of the input waves and observe the circuit limitations at low and high frequencies. You may observe a ringing response to the square wave; compare the period of the ringing to the characteristic time determined by your frequency response curve.

9.2.3 Logarithmic Amplifier

The circuit shown in Fig. 30 can be used to make a crude logarithmic amplifier. Note that this is a *non-linear* circuit (a sine wave in will not generate a sine wave out), so our analysis is restricted to the time-domain.

To understand why the output behaves as the log of the input, remember that the diode's I-V curve can be approximated as:

$$I = I_o(e^{V/V_T} - 1) \approx I_o e^{V/V_T} \tag{44}$$

where I_o and V_T are constants and V is the diode voltage; the approximation holds for $V > V_T$. Write the relation between V_i and V_o (remember that the inverting input is a virtual ground). If you plot V_o vs. $\log(V_i)$, you should get a straight line.

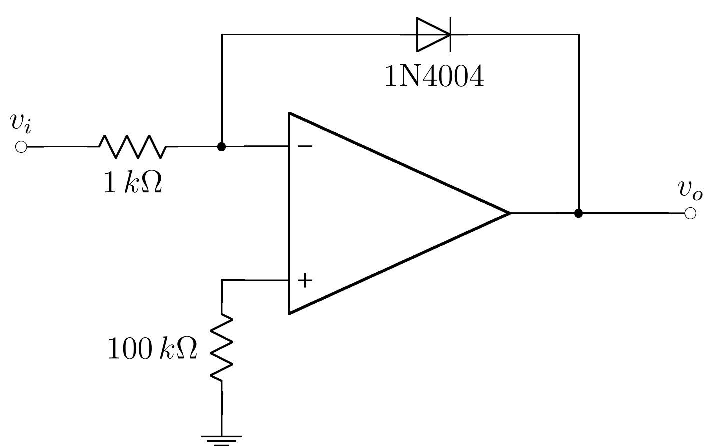

Figure 30: Logarithmic amplifier

1. Build the circuit shown in Fig. 30.

2. Use your Metex meter and the small variable DC voltage source to measure the response. From your plot, what values do you get for I_o and V_T? You can either plot the natural log of your data or relate the base-10 log to the natural log: $\log_{10}(x) = \log_{10}(e)\ln(x) = 0.4343\ln(x)$.

10 The Transition from Analog to Digital Circuits

Reference Reading: Chapters 6 and 7, Sections 6.8, 7.1, 7.2, 7.3 and 7.10.
Two lab periods will be devoted to this lab.
Goals

1. Be able to design and construct the following op-amp circuits:
   (a) A Summing Amplifier
   (b) A Digital to analog converter
   (c) A Transistorized logic switch
   (d) An Op-Amp Comparator and a Schmitt Trigger

10.1 Introduction

In this lab, we will connect the analog world we have been working in to the world of digital circuitry. For analog circuits, we often are concerned with the value of the voltage at an output. This voltage is often a function of the voltage at the input. However for digital circuits, a single output is used only to carry information which can be categorized as **TRUE** or **FALSE**. For example, a convention, called TTL or transistor-transistor logic, is often used: Any output voltage that is less than 0.5 volts is interpreted as meaning FALSE and any output voltage greater than 2.7 volts is interpreted as TRUE (voltage levels in between will be avoided). We could also use a 0 instead of FALSE and a 1 instead of TRUE (or even vise versa). Each input or output of the circuit represents a *bit* of information. The *bit* can only represent information which can be categorized as TRUE or FALSE such as the answer to *Has a button been pushed?* or *Is a switch in the ON position?*

With the use of several binary bits, we can represent numbers. For example, three bits can be used to represent any number from 0 to 7.

3 bit binary	000	001	010	011	100	101	110	111
decimal	0	1	2	3	4	5	6	7

Similarly 4 bits can represent 0 through 15, and so on.

Analog circuits can never be exact. For example, if you build an amplifier designed to produce an output voltage which is ten times its input voltage, the output will never be *exactly* ten times the input voltage. Furthermore, if you attempt to build two identical circuits, they will not produce *exactly* the same results because of differences in resistances, etc.

Digital circuitry does not have this problem. It is quite easy to build a circuit which takes a binary word as input and produces a binary output number which is *exactly* ten times the input number. If we build two identical (properly designed) circuits, they will produce identical results (we might find output bit 1 at 4.4V in one circuit and output bit 1 at 4.8V in the other circuit, but both of these represent TRUE or 1, so we consider this the same output).

We will start with a circuit that can convert a digital signal to an analog output. We have a set of allowed inputs, and want to make an analog output voltage that is proportional to the input setting. An example is a computer controlled device, where the computer can only set discrete values, but we want a varying voltage as output. We do this by using an op-amp circuit called a summing amplifier, and use this to build a so called *digital to analog converter*, DAC.

We will then begin building the components that allow us to construct a digital circuit. The first step in moving to digital circuits is to build a simple electronic switch which can represent a bit of information. To be useful this switch should yield one of two output voltages that are essentially equal in magnitude to the same two possible input voltages. That is, we want to process logical 1 as one voltage and logical 0 as another and we want to build logic circuits that combine inputs to yield answers to questions such as: *Are all inputs high?* (an AND circuit) or: *Is at least one input high?* (an OR circuit). A logical 1 should be the same voltage throughout the circuitry. As an example, we will build a transistor switch using a bipolar junction transistor that is either in the *off* or non-conducting state (which in this case generates a high output voltage) or in the *on* or fully conducting saturated state (which generates a low output). Similar switches can be (and usually are) built with FET/JFET/MOSFET transistors.

Next, we want to be able to take an analog signal (output of some detector or sensor) and ask a binary question of it: has the signal reached some pre-set threshold level? This operation is performed with a comparator. To do this in a stable way requires the use of *positive* feedback. This type of feedback accomplishes two things: 1) rapid output swings for slowly varying inputs and 2) hysteresis to avoid multiple transitions due to noisy input signals. You will build one type of *Schmitt trigger* circuit that accomplishes this.

10.2 Procedure

10.2.1 The Summing Amplifier

Build the following two-input summing amplifier. Use a DC source of 5V for the +5V. For the 0V,−1V input set your DS335 signal generator to a square wave of 1 Volt peak-to-peak and apply a voltage offset to produce a signal that switches between 0V and -1V.

Design the circuit so that you obtain an output square wave which alternates between 0 and −5 V. The zero-order analysis is all you need to design this circuit; the feedback current is just the sum of the currents generated in the input resistors and the negative input to the op-amp is a virtual ground. Verify that the output represents a weighted sum of the two inputs. You need to decide what the values of R_1, R_2 and R_f are. A good rule of thumb is that for inputs on the order of *volts*, we want currents in milliamps. Demonstrate that the output switches between the desired levels when the 0V,−1V level changes. Also verify that unplugging either of the two inputs has the expected effect.

(**Equipment note:** An obscure pathology has been noted in the interaction of the yellow

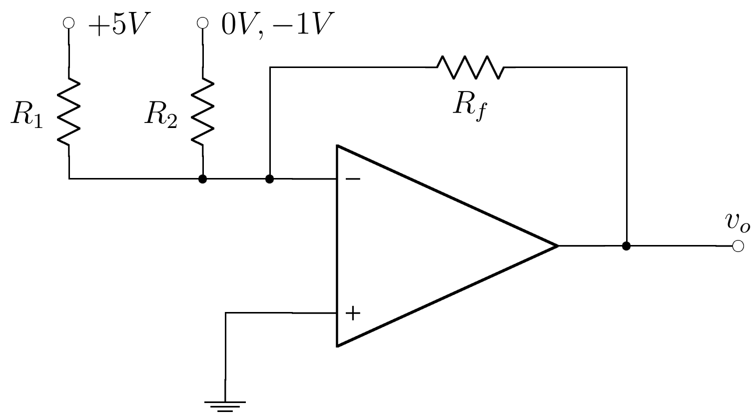

Figure 31: Voltage Summing Circuit

Metex multimeters with the 411 op-amp. Under certain conditions attempts to use one of the yellow multimeters to measure the DC output voltage of the 411 cause wild instability in the 411's output, visible if a scope is also connected, and causes a net DC offset to be measured by the meter. The brown multimeters seem to work fine.)

10.2.2 A 4-bit digital-to-analog converter (DAC)

Use the summing amplifier concept to build a DAC using your R-2R ladder circuit from early in the semester. In this example circuit, the digital side is set by mechanical switches (rather than a computer) and the analog output is at the op-amp output. The switches, which have been adapted so they plug into your proto-board) are *single pole, double throw*. *Single pole* means there is one *input wire*. *Double throw* means this input can be switched between two possible output terminals. Be sure you understand which pins are connected for each switch position before starting to connec up your circuit. In this circuit, a switch which connects the R-2R resistor to ground corresponds to a 0, whereas a switch which connects the R-2R resistor to *virtual ground* (the op-amp input), is a 1. Verify the DAC operation through the 2^4 switch settings. In your notebook, specify the bit corresponding to each switch.

10.2.3 Transistor Switch

Use a 2N3646 NPN transistor to build the simple digital switch of Fig. 33. The operation is as follows:

a) A 0 Volt input turns the transistor off since $V_B = V_E$ and the base-emitter junction is not forward biased. What is $V_C = V_o$ in this case?

b) A 5 Volt input strongly forward biases the base-emitter junction. Assuming the transistor is conducting, what is V_B? Assuming the transistor is in its linear operating range, what then would be the collector current if $\beta \approx 100$? What would $V_C = V_o$ be? Clearly, the transistor *must not* be in its linear range! In fact, the transistor reaches *saturation*

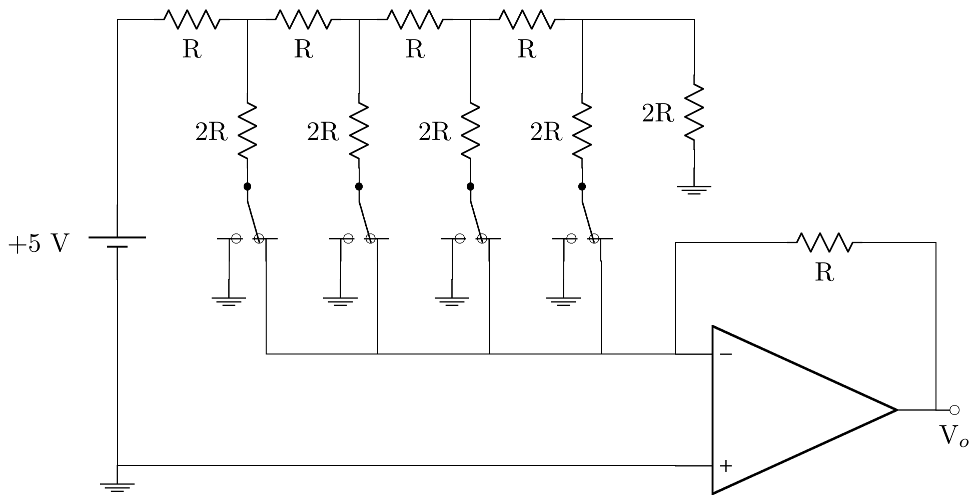

Figure 32: Digital to Analog Converter

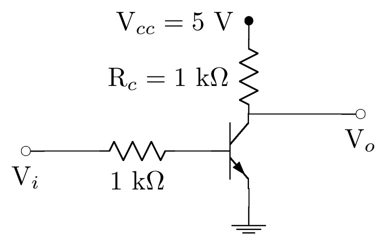

Figure 33: A transistor used as a binary switch

where the collector-emitter voltage is small and the collector current is limited by R_C rather than being calculated with the assumed β.

c) Somewhere between 0 Volts and 5 Volts input, the transistor is in its linear range. Here, the circuit is similar to the common emitter amplifier with $R_E = 0$. This means the gain is quite high and a small variation in V_i drives the output between the limits discussed above.

1. Build the circuit of Fig. 33. Use your adjustable DC supply for V_i and the proto-board supply for V_{cc}.
2. Measure V_o for 0 and for 5 Volt inputs and compare to your answers to the questions above.
3. Over what range of input voltages does the output switch states?
4. How fast can this switch operate? Here, use a $5\,V$ peak-to-peak square wave from the DS335 with a DC offset so that the voltage varies from 0 to $5\,V$ instead of ± 2.5 V. To how high a frequency does the output form a square wave? At very high frequency, can you see that there is a delay in turning the transistor off? Is there a corresponding

delay in turning the transistor on? Such delays are intrinsic limitations of *saturated logic* bipolar junction transistor circuitry.

10.2.4 Op-Amp Comparator

Build the comparator shown in Fig. 34 (left) using a 411 op-amp. In this circuit, an adjustable reference voltage V_{ref} is created using a *potentiometer*. The 411 op-amp is used to compare the input signal, V_{in}, with the reference voltage, V_{ref}. Since there is no feedback network, the op-amp goes to negative saturation as soon as $V_{in} > V_{ref}$ and to positive saturation when $V_{in} < V_{ref}$.

Check the behavior of this circuit by observing its output when a triangular waveform is used as the input (visualize both signals on the oscilloscope). Try varying V_{ref}.

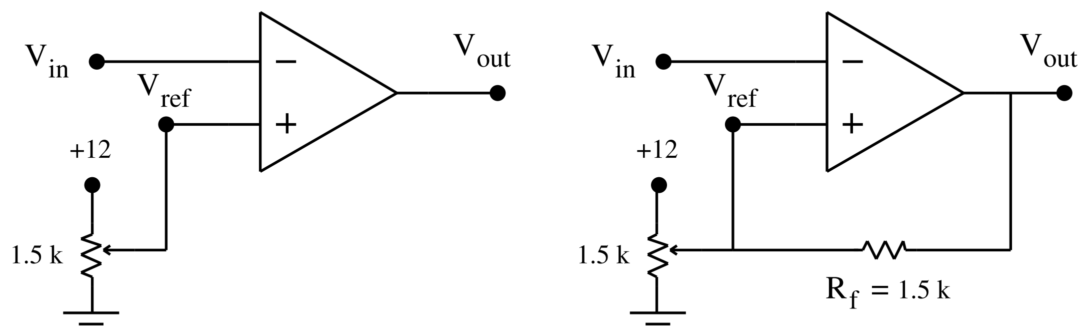

Figure 34: (left) Simple comparator built from an op-amp. (right) Comparator using positive feedback to implement a Schmitt Trigger.

10.2.5 Schmitt Trigger

The output of the comparator shown in Fig. 34 (left) is uncertain when $V_{in} \approx V_{ref}$ (i.e., it is very sensitive to the exact values). In actual use, we need to worry about what happens as our input signal crosses V_{ref}. In many applications, the input signal may be varying slowly (compared to the transition time of the circuit) and may be "noisy". In this case, the comparator could output a series of short pulses as the transition voltage is crossed. This is undesirable behavior.

Using *positive feedback*, we can build a circuit that minimizes this problem. *Positive feedback generates hysteresis*: once the output switches states, a small noise signal on the input will not cause the output to switch back. This handy detector circuit is call the Schmitt trigger.

Add the feedback resistor shown in Fig. 34 (right). Explore the behavior of this circuit using a triangular waveform for an input signal. Note how the reference voltage used to define the transition point for an increasing input signal is higher than the reference voltage for a decreasing signal. This is the characteristic of positive feedback used in the Schmitt

Trigger. Explain how this behavior can be used to avoid oscillations as a noisy input signal crosses the reference voltage level.

11 Digital Circuits and Logic Gates

Reference Reading: Chapter 7, Sections 7.4, 7.5, 7.6, 7.7 and 7.8.
Two lab periods will be devoted to this lab.
Goals

1. Become familiar with the operation of simple logic gates.
2. Be able to set up and use a flip-flop.
3. Understand what a switch de-bouncer does.
4. Be able to set up and use a 555 clock chip.
5. Be able to design and construct a digital counter.
6. Be able to construct a shift register circuit.

11.1 Introduction

In this lab, we will become familiar with logic gates and the use of more complicated logic circuits. We will also set up a clock circuit and use it to drive a counting circuit. The logic gates that we will be using come in rectangular packages called DIPs (dual in-line packages) as shown in Figure 35. The pin numbering scheme is standard over all such chips and is indicated in the figure. Not only will the IC have inputs and outputs related to the logic gates inside, it will also have an external power (V_{CC}) and ground connections. As with op-amps, these power connections are not typically shown in circuit diagrams, but are crucial to the operation of the chip.

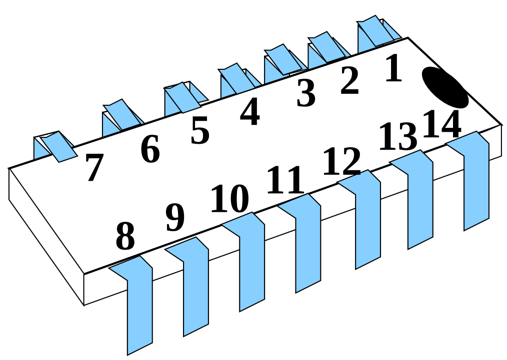

Figure 35: The pin numbering scheme on rectangular IC packaging. The *tab* as indicated by the dark oval in the diagram tags the end of the chip with the lowest and highest pin numbers.

11.2 Logic Gates

11.2.1 Procedure

In this section we will verify the functioning of simple logic gates. The operation of logic gates are specified by truth tables as shown in the text. In order to verify the operation of a gate it is necessary to measure the output for all possible combinations of inputs. In this section we will verify the truth table for the 7400 NAND gate and the 7402 NOR gates (pin-outs shown in Figure 37). The specifications sheets for these two gates can be found on the course web site. Note that the pin configuration for the two integrated circuits is **different**. You will find that each of the ICs that we use are so-called "quad packs", meaning that they each contain four independent gates. We will only need to measure one of the gates in each IC.

While we could simply test this with a $5\,V$ power supply and a DVM, we will build a somewhat more sophisticated circuit for this. We will us a $5\,V$ DC power supply and a single ground connection to power the IC. We will also use the $5\,V$ supply to provide the logic signals to the IC. To do this, we will us a pair of *single pole double throw switches* (SPDT) to switch the gate inputs between the supply level and ground. It is important to note that for logic inputs we must use either $5\,V$ or $0\,V$. We cannot simply let an input float if we want $0\,V$. The correct wiring is indicated in Figure 36.

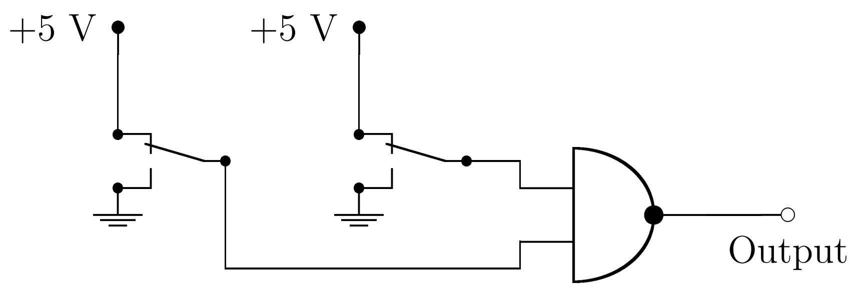

Figure 36: Two single pole double throw switches which are used to control the input to a NAND logic gate. The output is then measured to the right of the gate.

You could use either the scope or an LED to observe the output. In this lab, we will measure the output of the logic gate using an LED. When using LEDs to observe the output of TTL logic, be sure to put them in series with current-limiting resistors. This limits the maximum current to around $10\,mA$ and will protect the output ports of the gates. Such a circuit is shown in Figure 38, we can have the LED on either when the output is high or when it is low, depending on which configuration we use. In fact, we could also connect LEDs to the two inputs to the gate as well. In such a case, we could easily read off the truth table for our logic gates.

Use the circuits to measure the truth tables for both the NAND and NOR gate as indicated above. Demonstrate that it agrees with what is listed in your text book.

In order to see how fast these ICs are and how clean the signals are at high frequency, replace one of the switches with the DS335 (5V peak-to-peak, 2.5V offset square wave) and

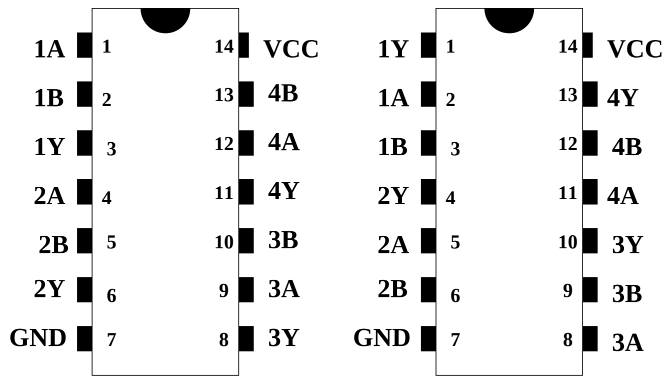

Figure 37: The pin-out of the 7400 (left)and 7402 (right) chips. These each have four gates, with inputs A and B and output Y. Note that they are not pin compatible.

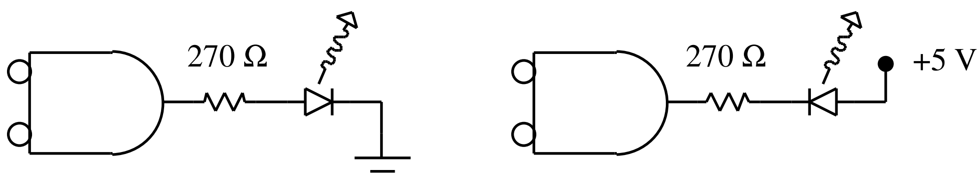

Figure 38: Current limiting resistors should be used in series with LEDs. (left) LED lights when output high. (right) LED lights when output low.

drive the circuit at high speed. Tie the second input either to ground or to 5V so that the DS335 switches the output. Then look at the output on your scope. Can you deduce a rough estimate for the maximum clock rate at which such circuits can be used?

11.3 RS Flip Flops

A flip-flop circuit is a *memory circuit*. It can be set into two possible output states. A common holding input will then keep both of these output states until some input changes. In this sense, the flip-flop can hold one *bit* of information—either a 0 or a 1. The simplest of the flip-flop circuits is an RS flip-flop. In an RS flip-flop, the R stands for *RESET* and the S stands for *SET*. They can be thought of as either SETting the output to 1 or RESETting the output to 0.

11.3.1 Procedure

An RS flip-flop can be built using two NAND gates as shown on the left-hand side of Figure 39. While the circuit diagrams in this section look deceptively simple—no resistors, no capacitors, no inductors—they are not. You will find it necessary to be very careful in wiring the circuits as there are lots of wires and interconnections. At this point, we will note that a NAND and an inverted OR are the same thing. This amounts to an application of DeMorgan's theorem. If you switch where the inverting circles are (between inputs and outputs) and switch between OR and AND, you have the same thing you started with. Show that the truth table for both a NAND gate and an inverted OR gate are the same.

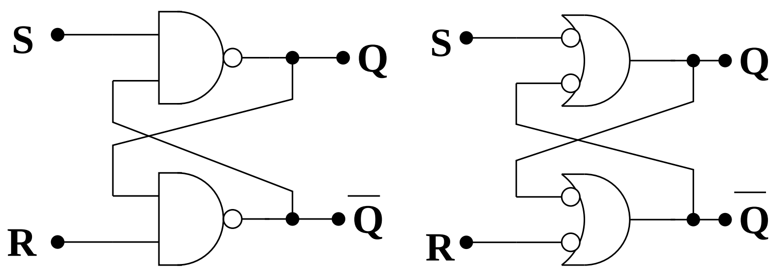

Figure 39: The left-hand circuit shows an Reset-Set (RS) flip-flop built from two NAND gates. By DeMorgan's Theorem, this can be shown to be logically equivalent to the circuit on the right which has the negated R and S going into two OR gates.

We will now build an RS flip-flop using the 74xx00 NAND gate that we used earlier. Don't forget to wire up the $+5\,V$ and ground to your gate. SETing this circuit makes the Q output high (and the $\overline{Q}$ output low). RESETting reverses this. Keeping the SET and RESET signal off (which means at the supply voltage) leaves the circuit in it's previous state. So the *normal* state of the circuit is to have both inputs high. In this state, the output remembers which input was last toggled from high to low and back to high again. Any number (≥ 1) of such toggles yields the same output. As soon as the opposite input is toggled to low, the output switches and stays the same when this input is returned to the high state.

You can use the switch set-up you used above to toggle the inputs to low and back to high. Verify the memory feature of this circuit and the ability to set outputs to a desired state. Write out the values of the four inputs to the two gates, for each of the four possible SET/RESET input combinations. What happens when both the SET and RESET signals are present at the same time? (Demonstrate the memory effect of this circuit.)

A Switch De-bouncer When we use a switch in a circuit, we nominally assume that its output will be a *perfect* step function. Either going from low to high or from high to low, and then remaining. Unfortunately, the mechanical nature of many switches leads to a situation where the process of mechanically opening or closing a switch actually causes the switch to *bounce*, and the output oscillates many times before settling in to the desired state. In many situations, this is not desirable. An RS flip flop can be used to *de-bounce* a switch. Once a RS flip-flop has changed states, it will not change back unless the other input is toggled. Because a switch does not actually bounce back and forth between the two inputs, we can use an RS flip-flop to ignore the bounce. Such a circuit is shown in Figure 40.

Build the de-bounce circuit shown in Figure 40 and demonstrate that it does function as a switch. To see the de-bouncing effect, you can look at the input to the Set on one scope trace and the Q output on the other. Note what you observe in your lab book.

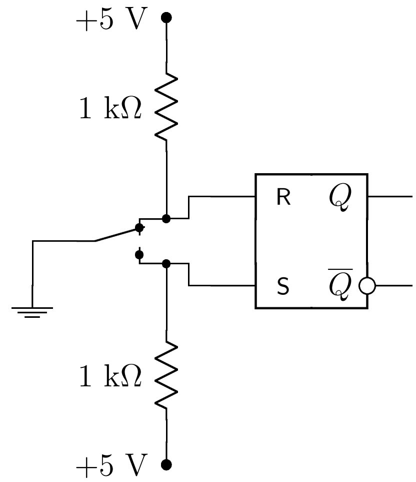

Figure 40: An RS flip-flop used to de-bounce the output from a switch. Once the flip-flop changes state, it will remain in the new state, independent of whether the switch bounces.

11.4 Clocks

Digital electronics does not normally sit in some fixed state, but rather performs logic operations on input to produce output. The rate at which these operations are performed is defined by an external clock. A typical processor chip for a computer has a rating that is in GigaHertz that indicates the clock speed. While we will not be doing such high-speed electronics, we will set up a clock in this lab and then use its output to drive a circuit. We will us a so-called 555 chip for this. This is a very common chip whose pin-out has been standardized over all vendors. This is shown in Figure 41. For a detailed discussion, see section 7.6 in your textbook. The basic idea is to use an RC circuit to define a characteristic time, τ_{RC}, at which the clock *ticks*. However, we have somewhat more control in that we can also control what fraction of the clock period which is high and that which is low, f_{high} and f_{low}.

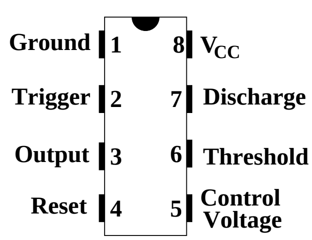

Figure 41: The pin-out of the 555 clock chip.

This functionality can be achieved using two resistors and a capacitor which are hooked up externally to the 555. The appropriate circuit is shown in Figure 42. In terms of R_1, R_2 and C, it can be shown that the period of the clock is

$$T_{555} = \ln(2)\,(R_1 + 2R_2) \cdot C\,.$$

The ln(2) comes from the exponential decay of an RC circuit and what fraction of the characteristic time it takes to fall below some threshold. In addition to the period, we have the high and low fractions. These are given as

$$\begin{aligned} f_{low} &= \frac{R_1 + R_2}{R_1 + 2R_2} \\ f_{high} &= \frac{R_2}{R_1 + 2R_2} \end{aligned}$$

which are an apparent voltage divider.

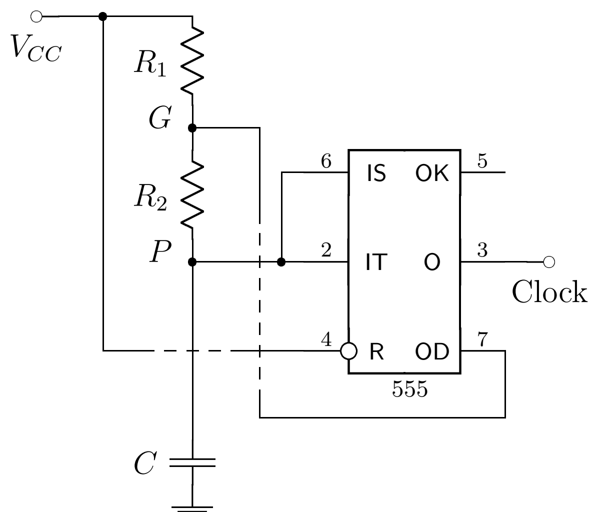

Figure 42: A 555 clock IC in a circuit to produce a clock output signal with period $T = 0.693 \cdot (R_1 + 2R_2)\, C$. The output is on the *Clock* line.

11.4.1 Procedure

Before proceeding, we note that you will be using the clock circuit in this part of the lab to drive the circuits in the next two sections. **DO NOT DISASSEMBLE YOUR CLOCK CIRCUIT.** It is also advisable that you try to build your clock circuit as close to one end of your proto board as possible. Otherwise, you will run out of board real estate later in the lab.

In this lab, we would like to set up our 555 chip to have a period of about 1 second and to have the low fraction be about twice the high fraction. Before starting, use the high and low fractions to find the relative size of the two resistors. Using the relation that you derived, it is possible to calculate the needed capacitance for a specified resistance to yield the correct period. Work out several possible values that use different orders of magnitudes of the capacitance, (*e.g* μF, 10s of μF, 100s of μF and 1000s of μF. Based on the values you get, justify your decision for your final choice.

At this point, inventory the capacitors that are available in lab. Choosing one that we have, determine the values of the needed resistances and see how close you can get to them. Once you have all your components (measured), build the circuit shown in Figure 42 and measure its output. Does it have the expected period. Finally, add an LED to the output of your clock chip (Figure 38) and let the lights flash.

11.5 The Binary Counter

In addition to the RS flip-flop, there are other types of flip-flop circuits. In this section, we will use a so-called JK flip-flop (see section 7.5.2 in your textbook) to build a counting circuit. The JK flip-flop has three main inputs, J, K and a *clock*. It also has a clear which allows it to be put in some default state.

Depending on the levels at the J and K inputs, the rising edge of the clock (or the falling edge, in some chips) causes the output Q to change. The truth-table for the JK flip-flop is shown in Table 1. We first note that CLR is high (or in the table, the NOT CLR is low), the flip-flop is put into a default state. In normal operation, the CLR is low (the NOT CLR is high). In normal operation, if both J and K are low, then clocking the circuit leaves the Q and $\bar{Q}$ outputs unchanged. If one of J or K is high, and the other is low, then Q is set to the value of J and $\bar{Q}$ is set to the value of K. If both J and K are high, then clocking the circuit causes Q to be set to what $\bar{Q}$ was before the clock pulse, while $\bar{Q}$ will be set to the former value of Q. In this mode, we say that it *toggles* the value of Q. In this lab, we will be using the 7473 chip which has a "NOT CLR" input. The truth table for this chip is given in Table 1.

$\overline{CLR}$	CLK	J	K	Q	$\bar{Q}$	Comment
L	x	x	x	L	H	Default
H	falling	L	L	Q_{n-1}	$\bar{Q}_{n-1}$	Hold
H	falling	H	L	H	L	Set
H	failing	L	H	L	H	ReSet
H	falling	H	H	$\bar{Q}_{n-1}$	Q_{n-1}	Toggle

Table 1: The truth table for the JK flip-flop. In this case, the flip-flop responds to the falling edge of the clock pulse.

In the toggling mode (both J and K high), it is easy to show that the output changes state at one-half the frequency of the clock input. We will take advantage of the toggling output mode to build a digital counter circuit. The basic idea being that output of one JK flip-flop will serve as the clock input to the next one. As such,each subsequent flip-flop will be clocked at one-half the frequency of the previous one.

11.5.1 Procedure

We will use the 7473 dual JK flip-flop (spec sheet is on the course web site) to build an eight-bit binary counter(pin-out shown in Figure 44). We will use the 555 clock circuit that you set up earlier as the clock input to our circuit.

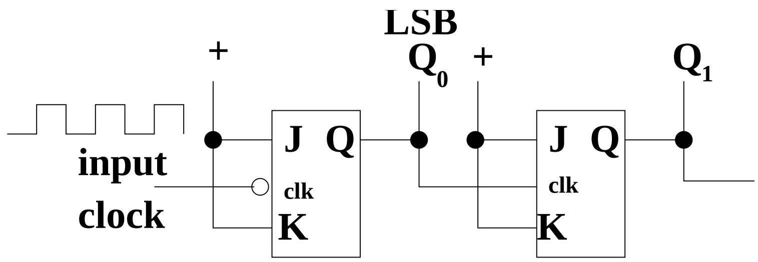

Figure 43: A two-bit binary counter built using JK flip-flops. This can easily be extended to more bits.

Start by setting up the circuit shown in Figure 43 for a two-bit counter. You will find that the 7473 is a dual-pack (it has two flip-flops on a single chip). Hook the outputs, Q_0 and Q_1 to LEDs as done earlier in the lab. Use the 555 circuit that you set up as the clock input for the counter. Once you have verified that the circuit is indeed counting, add six more bits to your circuit to build an eight-bit counter.

You could also try using a switch, rather than your 555 clock, for the input to the counter. However, you would find that switches produce erratic output due to *contact bounce* as discussed above. The counter (or any logic circuit) may see many logic pulses, rather than a single pulse, as the mechanical switch makes or breaks contact. This is one example where the de-bouncer discussed above can be used as input to the circuit. Such a de-bouncer circuit is commonly used on 'momentary' push-button switches which change state when they are pressed and released.

11.6 The Shift Register

A shift register is a circuit that shifts bits by one bit on each input clock pulse. Section 7.8 of your text book shows how a simple shift register can be built using D flip-flops. In this section, we will use an SN74LS164, which is an 8-bit shift-register chip, rather than building our own. The pin-out for this chip is shown in Figure 44 and it's truth table is given in Table 2.

The shift-register has four inputs and eight outputs. The clock input is labeled CP and there is a reset input labeled $\overline{MR}$. If the reset is pulled low, then all of the outputs ($Q0$ to $Q7$) are set to zero. As long as the reset is held high, the shift register will clock the bits from lowest ($Q0$) to highest ($Q7$), with one shift on each clock pulse. Finally, there two inputs A and B allow one to set the lowest bit high. As long as one of these (A or B) is held low, $Q0$ will not be set. If both are high, then $Q0$ will go high on the next clock pulse.

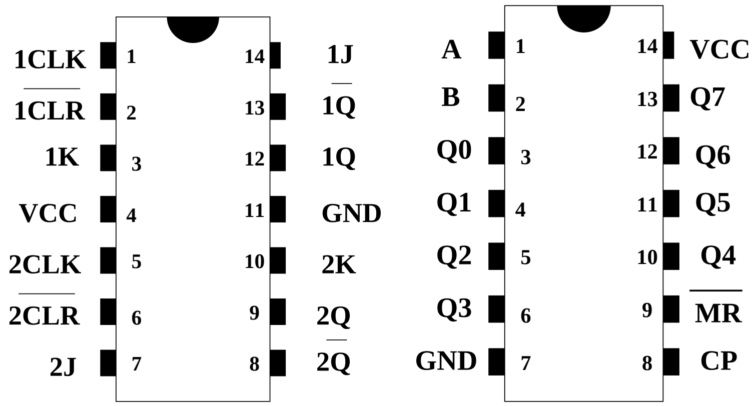

Figure 44: (Left) The pin-out of the SN7473 JK-flip-flop chip. (Right) The pin-out of the SNLS164 8-bit shift register chip. Both the A and B inputs need to be high to set $Q0$. CP is the clock input and $\overline{MR}$ is the master reset. The outputs are $Q0$ through $Q7$.

Operating	Inputs			Outputs	
Mode	$\overline{MR}$	A	B	Q0	Q1-Q7
Reset	L	X	X	L	L-L
Shift	H	L	L	L	Q0-Q6
	H	L	H	L	Q0-Q6
	H	H	L	L	Q0-Q6
	H	H	H	H	Q0-Q6

Table 2: The truth-table for the SN74LS164 8-bit shift register. If the reset line goes low, the chip is reset. If the reset is high, then the contents of Q0 to Q7 are clocked through the shift register. If both A and B are high, then Q0 is turned on during the clock pulse.

11.6.1 Procedure

In this section, we are going to set up an eight bit shift register which is driven by the 555 clock circuit from above. Each of the eight bits needs to be connected via an LED to ground. We will then connect the B input to V_{CC} and use a single pole double throw switch to toggle the A input between ground and VCC (see Figure 36). Finally, we need to connect the reset ($\overline{MR}$) to V_{CC}. To each of the eight outputs, connect an LED as we did in the left-hand circuit of Figure 38.

It is advisable that you sketch the circuit which you want to build in your lab book before starting. You will also need to lay out the real estate on you circuit board carefully so that things fit.