Lab 13: Voltage Multipliers

Reference Reading: Chapter 4, Sections 4.6
Time: One and a half lab periods will be devoted to this lab.
Goals:

1. Understand how buffering capacitors can be combined with diodes to clamp a voltage to a DC level.
2. Understand of a half-wave rectifier combined with a buffering capacitor can be used to obtain a DC voltage from an AC input.
3. Understand how these elements can be combined to build a multi-stage voltage multiplier.

13.1 Introduction

In this lab we will work with simple diode-based circuits to understand how to take an AC input voltage and produce a DC output whose voltage is larger than the amplitude of the input voltage. We will ultimately use this to build a Cockroft-Walton voltage multipler, and then we will examine the output characteristics of this multiplier.

13.1.1 The Voltage Clamper

The voltage clamper is a circuit that will add a constant DC offset to an AC signal. A simple example of this circuit is shown in Figure 13.1 where the DC offset is created by charging up a buffer capacitor, C, in the circuit. We will start by assuming that the voltage drop across the diode

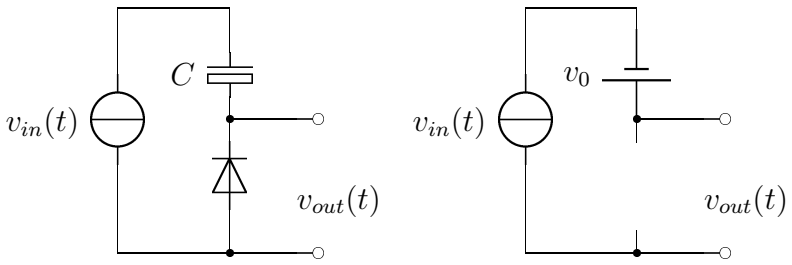

Figure 13.1: The left-hand circuit shows a voltage-clamper. After the capacitor charges up to the amplitude of the input voltage, v_0, current is no longer able to flow in either direction across the diode. The right-hand circuit shows what effectively happens after the capacitor is charge. The diode behaves as if it is not there and the capacitor looks like a DC voltage supply.

is zero, $V_d = 0$. Then, assuming that we have an input voltage of

$$v_{in}(t) \quad = \quad v_0 \cos(\omega t) \ ,$$

which we can write in terms of the period T as

$$v_{in}(t) \quad = \quad v_0 \cos\left(\frac{2\pi t}{T}\right) \ .$$

The capacitor will eventually charge up so that there is a voltage v_0 across it with the lower side being at a higher potential than the upper side. Hence, the orientation of the electrolytic capacitor in Figure 13.1. This leads to an output voltage of the form

$$v_{out}(t) \quad = \quad v_0 + v_0 \cos\left(\frac{2\pi t}{T}\right) .$$

We can see this by assuming that the lower side of the voltage source is at a higher potential than the upper side. Then the diode will be forward biased and current will flow up through the diode and the capacitor. Thus, the lower side of the capacitor will be at a higher potential than the upper side. If the upper side of the voltage source now has the higher potential, then the diode will be reverse biased and no current will flow. Thus, to the extent that the time it takes to charge and discharge the capacitor is long compared to the period of the voltage, the capacitor will charge up, and in doing so the output voltage will be clamped to voltage of the capacitor. Such a rising voltage is shown in Figure 13.2 where we see the capacitor start to charge up at time $t = 0$, and then charge up over several periods of the input voltage.

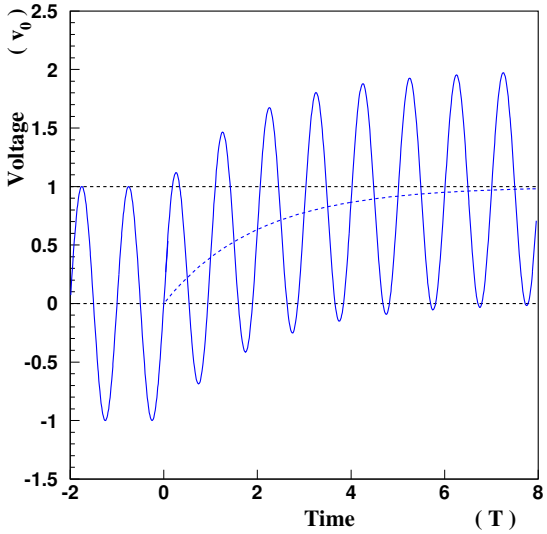

Figure 13.2: The output of a voltage clamper. At time $t = 0$ the capacitor begins to charge up, eventually pulling the DC level on the output up to v_0.

The rate at which the capacitor charges up is controlled by an RC time constant, τ_{RC}. In the circuit in Figure 13.1, there is no obvious resistor in the circuit. However, we note that the AC supply driving the clamp has some output impedance, Z_{out}. The magnitude of this Z_{out} will serve as the resistance R in our circuit. If the circuit is driven by an input voltage of amplitude v_0 and the DC voltage sags to v_s over one period of the input signal, then we can write that

$$\frac{v_s}{v_0} \quad = \quad e^{-T/\tau_{RC}} ,$$

where we recall that the characteristic time is given as

$$\tau_{RC} \quad = \quad RC\,.$$

Thus, we can write that

$$\tau_{RC} \quad = \quad -T \,/\, \ln\left(\frac{v_s}{v_0}\right)\,. \tag{13.1}$$

For the voltage to drop to no less than 95% of the input voltage, we must have that $\tau_{rc} \approx 20\,T$ and for no less than 99% of the input voltage, $\tau_{rc} \approx 100\,T$.

There is one last effect which we need to look at not. We assumed that there was no voltage drop across our diode, $V_d = 0$. In general, this is not true. If v_0 is large in comparison to V_d, this may be a reasonable approximation, but we will examine the case when this is not necessarily true. Our idealistic approach to treating a diode is to take V_d as a constant (typically $0.65\,V$). Under this assumption, we would just expect that the DC level would go to $v_0 - V_d$ and everything else that we did above is correct. This is a good first approximation, but in fact it is not completely correct.

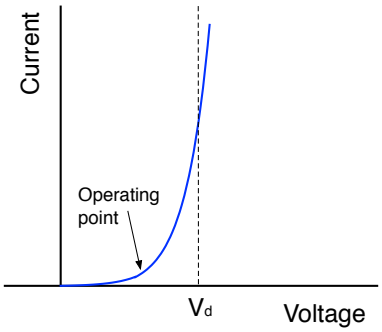

Figure 13.3: The I-V curve of a diode following equation 13.2.

We saw that we could describe the I-V curve of a pn-junction (or a diode) as an exponential function where

$$I(V_d) \quad = \quad I_S\left(e^{V_d/V_T} - 1\right)\,. \tag{13.2}$$

In this expression, the thermal voltage V_T is just

$$V_T \quad = \quad \frac{k_B T}{e}\,,$$

and is approximately $25\,mV$ at room temperature. The saturation current, I_S is just a constant value. We can solve equation 13.2 to give that

$$V_d \quad \approx \quad V_T \ln\left(\frac{I_d}{I_S}\right) \tag{13.3}$$

In Figure 13.3 we show the expected I-V curve of a diode. There we see that the nominal voltage drop, V_d is chosen to be an average for typical operating currents in the diode.

As the capacitor charges up to the nominal diode voltage, the amount of current that can flow to continue the charging decreases. This in turn causes a logarithmic drop in the value of the diode voltage, V_d as we move down the curve in Figure 13.3. In the end, the capacitor will actually be able to charge up beyond our nominal expectations, and we will have a smaller than expected voltage drop across the diodes. This is indicated as the "Operating point" in the Figure.

13.1.2 The Voltage Doubler

The voltage doubler circuit adds a half-wave rectifier to the output of our voltage clamp from Section 13.1.1. This rectifier then uses a second capacitor to buffer the output such that it will charge up to twice the input voltage, $2v_0$. In the left-hand circuit in Figure 13.4 is shown the simple voltage doubler. Assuming that we have chosen reasonable values for our capacitors, the voltage clamper charges up to v_0, meaning that the point between the C_1 and the two diodes will have a voltage given as

$$v(t) \quad = \quad v_0 \left(1 + \cos \omega t\right) . \tag{13.4}$$

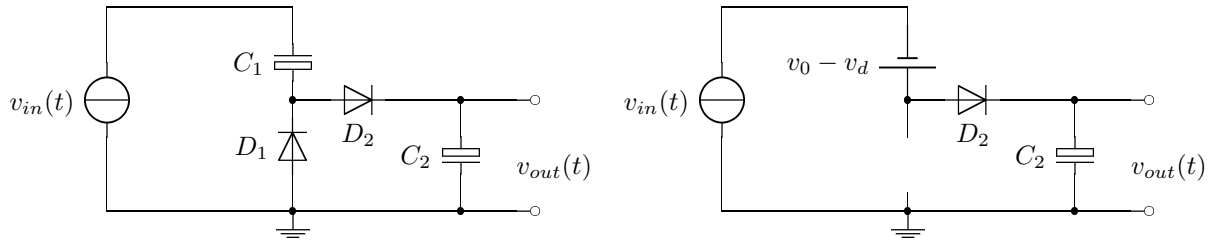

Figure 13.4: On the left is shown a voltage-doubler circuit. The first capacitor/diode pair (C_1 and D_1 form a voltage clamper, which then drive the half-wave rectifier formed by D_2 and C_2. Once C_1 charges up, it will behave like a DC voltage source of value. This also leads to a situation where D_1 no longer allows current to flow in either direction. This means that the circuit will behave like that shown in the right-hand schematic.

When this happens, diode D_1 effectively stops conducting in either direction, so we can pretend that it is no longer present (as we did in the right-hand side of Figure 13.1). Because C_1 is charged up to a voltage v_0, we can treat it as a DC voltage source. Thus we can draw the equivalent for our doubler as in the right-hand circuit in Figure 13.4. The diode D_2 will now conduct when the upper side of the voltage source is more positive than the lower side, and as we saw with the clamp. This means that the capacitor C_2 will charge up. It will eventually reach a point when it has a voltage of $2v_0$ across it, with the upper face being more positive than the lower face. When this happens, the diode D_2 will no longer conduct in either direction. As such, we will be left with a constant DC voltage of $2v_0$ across the capacitor C_2. Thus, the output will be a DC voltage whose values is twice the amplitude of the inputs AC signal.

$$v_{out} \quad = \quad 2\, v_0 \, .$$

We now note that the above discussion assumed that the voltage drop across our diodes was zero, $V_d = 0$. As it is not, we expect that the output voltage will be lower by two diode drops, or

$$v_{out} \quad = \quad 2\, v_0 - 2\, V_d \, .$$

We now recall that as we saw with the voltage clamper, we do not see the full V_d drop across the diodes, but only some fraction of it. We therefore expect the voltage to be between the above expression and $2v_0$.

While we have built a circuit that appears to have a DC level that is twice the input, in fact there are some issues which limit this circuit. In particular, the output impedance of the circuit

tends to be fairly large and the voltage doubler cannot supply very much current to a load. We will investigate this further when we discuss the voltage multiplier in Section 13.1.3.

13.1.3 The Voltage Multiplier

We can continue with the doubler circuit that we examined in Section 13.1.2 by adding additional stages to the circuit. Such a circuit is shown in Figure 13.5 where the output labeled a corresponds to the doubler we saw earlier. There we saw that

$$V_a \;=\; 2\,v_0 - 2\,V_d$$

where v_0 is the amplitude of the input voltage, $v_{in}(t)$, and V_d is some fraction of the nominal voltage drop across one of our diodes. The second stage has an output at b and has a nominal output voltage of

$$V_b \;=\; 4\,v_0 - 4\,V_d\,.$$

The third stage has its output at c with nominal output voltage of

$$V_c \;=\; 6\,v_0 - 6\,V_d\,,$$

and if we were to continue this circuit to n stages, we would expect that output voltage V_o would be

$$V_o \;=\; 2n\,(\,v_0 \,-\, V_d\,)\,. \tag{13.5}$$

This type of voltage multiplier is known as a *Cockroft-Walton voltage multiplier* and is named for its inventors, Sir John Douglas Cockroft[1] and Ernest Thomas Sinton Walton[2].

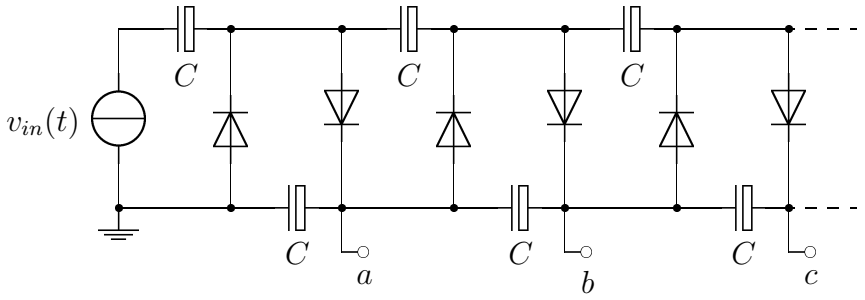

Figure 13.5: The Cockroft-Walton voltage multiplier.

While the Cockroft-Walton multiplier can be used to generate large DC voltages, it is rather limited in the current that it can deliver to its load. It also has an AC ripple on the nominal DC voltage level. Assuming that the multiplier is built using identical capacitors and diodes, the voltage drop from the nominal output voltage in equation 13.5 is given as

$$V_{drop} \;=\; Z_C\,I_L\left(4n^3 + 3n^2 - n\right)\,, \tag{13.6}$$

[1]Sir John Douglas Cockroft was a British physicist who worked with Ernest Rutherford in Manchester. He shared the Nobel prize in physics in 1951 with Ernest Thomas Sinton Walton for splitting the atomic nucleus.

[2]Ernest Thomas Sinton Walton was an Irish physicist who together with SIr John Douglas Cockroft developed the Cockroft-Walton accelerator that won them the Nobel prize in 1951 for the splitting of the atomic nucleus.

where Z_C is the magnitude of the impedance of one of the capacitors at the AC frequency f,

$$Z_C \;=\; \frac{1}{\omega C}\,,$$

and I_L is the current drawn by the load on the output of the multiplier. In literature, one often sees equation 13.6 approximated with $Z_C = 1/(6fC)$.

In addition to the voltage drop, the output also has an AC ripple whose amplitude, v_r, is given as

$$v_r \;=\; Z_C\, I_L\, n\, (n+1)\;, \tag{13.7}$$

where as before, the number of stages in the multiplier is given as n. This ripple voltage is the result of the capacitors charging and discharging and is shown schematically in Figure 13.6.

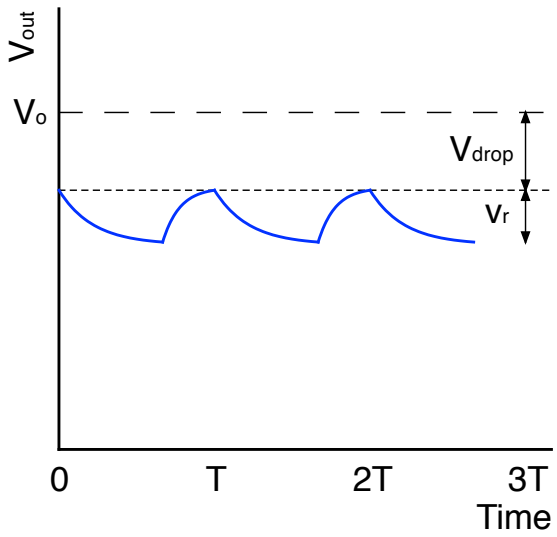

Figure 13.6: The output voltage of a Cockroft-Walton voltage multiplier. The nominal voltage V_o is given as in equation 13.5, the voltage drop under loading, V_{drop} is from equation 13.6 and the voltage ripple, v_r is given in equation 13.7. The ripple voltage arises from the charging and discharing of the capacitors under load.

We can use equation 13.6 to characterize the output impedance of the multiplier. We have that the output voltage under load of the multiplier is

$$V_L \;=\; V_o - V_{drop}\,,$$

which we can rewrite as

$$V_L \;=\; V_o - Z_C\, I_L \left(4n^3 + 3n^2 - n\right)\,.$$

From this, we expect that the output impedance, R_{out}, of the multiplier is given as

$$R_{out} \;=\; Z_C \left(4n^3 + 3n^2 - n\right)\;, \tag{13.8}$$

which increases rapidly (n^3) with the number of stages in the chain. We also saw that the ripple voltage increases as n^2 with the number of stages, thus without doing something additional, there is a very finite limit in the number of stages that make sense in such a voltage multiplier. Some discussion of tuning the capacitors to improve this performance can be found in the literature [3]. There, a more optimal solution is found when the the capacitors in Figure 13.7 are chosen based on the stage number, i.

$$\begin{aligned} C_{2i} &= (n-i+1)\,C \\ C_{2i-1} &= (n-i+1)^2\,C \end{aligned}$$

In such a configuration, the larger capacitors are in the earlier stages.

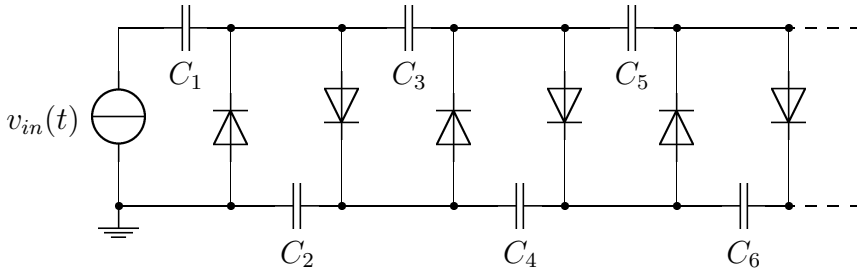

Figure 13.7: A more optimized Cockroft-Walton voltage multiplier.

13.1.4 Switched Capacitor Circuits

In the previous sections we have looked at ways of multiplying a AC voltage to produce a DC output. It would also be useful to be able to double a DC voltage directly. One way to do this is through circuits which use capacitors and switches. A simple example would be to charge two capacitors in parallel, and then switch them so that the output views the capacitors in series, thus doubling the voltage. A common method to achieve this doubling is through *charge pumping* where a capacitor is charged up, and then switched into a mode where it can transfer charge to a second capacitor. In that light, we will look at the *switched capacitor charge-pump voltage doubler* as shown in Figure 13.8.

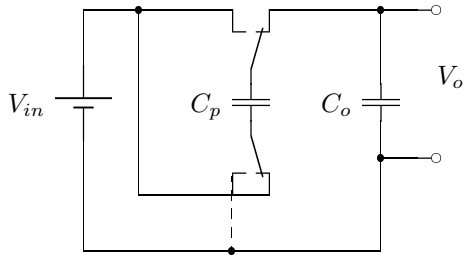

Figure 13.8: A switched capacitor charge-pump voltage doubler.

The two switches can either both be to the left or both to the right, and while we show these as a mechanical style switch in the diagram, in reality they are a pair of transistor switches whose

[3] See for example the article by I. C. Kobougias and E. C. Tatakis in the IEEE Transactions on Power Electronics, Vol. 25, No. 9, page 2460 (2010).

switching is controlled by an external clock. We can examine in detail the two possible states of the circuit, and show these explicitly in Figure 13.9 The left-hand picture shows the circuit when both switches are to the left, while the right-hand one shows both switches to the right. When

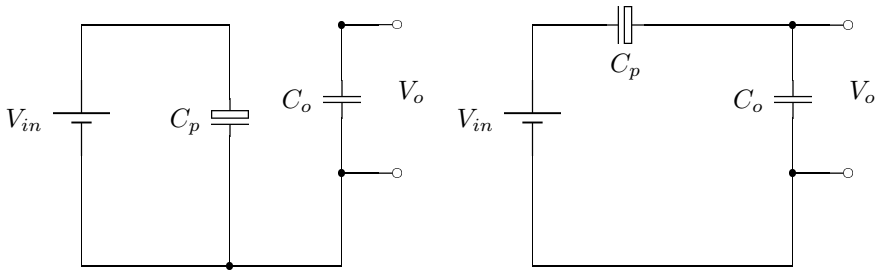

Figure 13.9: A switched capacitor charge-pump voltage doubler showing the two circuit configurations depending on how the switches are set. The left-hand circuit shows the capacitor C_p being charged up, while the right-hand circuit shows the output capacitor, Co being charged. Note that C_p is shown as an electrolytic capacitor to indicate which side is at a higher potential.

both switches are to the left, the capacitor C_P will charge up until it has the input voltage across it. We have shown it as an electrolytic so we can see which side (the upper) of C_P is at higher potential. In this mode, we also see that the output is just taken across the capacitor C_o. When the switches move to the right, we are in a state where C_o is being charged by both the input voltage V_{in} and the charged up C_P in series. This is similar to what we saw with the voltage doubler in Section 13.1.2 where the charged capacitor will behave like a DC voltage supply. This means that C_o will charge up to a voltage of $2V_{in}$. In this mode, we also take the output across C_o. After a sufficiently long time, we will have that $V_o = 2V_{in}$.

As noted above, the switches in these circuits are solid state based and controlled by a clock. This is typically accomplished by building an integrated circuit based device which has both the clock and the switches in it. External capacitors are then connected to this circuit. There are a rather large number of these available commercially. Here, we show how one of these is hooked up to form a voltage doubler in Figure 13.10. The pin out here is based on the LM2681 chip, but the same sort of external connections apply to all of these. In looking at the specification sheets for these devices, they typically can also be used to cut a voltage in half, or to invert a DC voltage. It is also possible to chain several of these together to obtain even larger multiplication of voltages. The interested reader is invited to consult the specification sheets for these devices[4].

[4]A very incomplete list of these include the LM2681, LM 2662 and LM2663 from Texas Instruments and the MAX1044, the MAX1682 and the MAX1683 from Maxim.

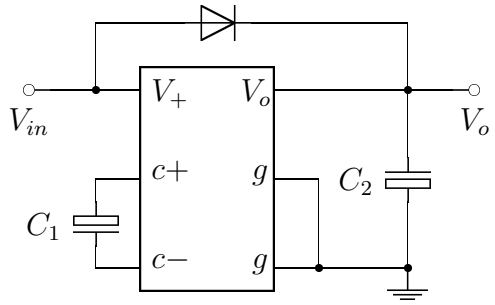

Figure 13.10: An integrated circuit voltage doubler with external capacitors and diode. The pin out shown is for the LM2681 switched capacitor voltage convertor. The input V_+ connects to the input voltage. The $c+$ and $c-$ inputs are for an electrolytic capacitor, C_1, while the g inputs both must be grounded. The output is taken from the V_0 terminal.

13.2 Preliminary Lab Questions

The work in this section must be completed and signed off by an instructor before you start working on the lab. Do this work in your lab book.

1. Consider the voltage clamper in Figure 13.1 and assume that V_d is zero. Sketch the input voltage, $v_{in}(t)$ and the voltage across the diode, $v_{out}(t)$ over one period before the capacitor has started to charge. Sketch the voltage across the capacitor over the same time period. Be sure to account for the orientation of the capacitor in your sketch.

2. Given the clamped voltage as in equation 13.4, sketch the voltage across the diode D_2 in Figure 13.4 before C_2 starts to charge up. Make your sketch for one period of oscillation, T.

3. Given equation 13.6, estimate the number of stages n before the voltage drop is equal to the nominal voltage. Assume that n is large enough that you only need the leading term and express your answer in terms of V_o, Z_C and I_L.

13.3 Equipment and Parts

In this lab we will utilize the following equipment. This equipment is located at your lab station.

1. The Tektronix TDS 2012B digital oscilloscope.
2. Two P2220 probes for the oscilloscope.
3. One USB memory stick which is no larger than 2GB.
4. The Stanford Research Systems DS335 signal generator.
5. One BNC to alligator cable.
6. The Metex 4650 digital meter.
7. The Global Specialities PB10 proto-board (see Appendix **??** for a description).

You will also need the following components in order to carry out this lab. It makes more sense to get them as you need them, rather than all at once before the start of the lab.

1. Eight 1N4004 diodes.
2. Eight $50\,V$, $1\,\mu F$ electrolytic capacitors.
3. One $47\,k\Omega$ resistor.
4. One $100\,k\Omega$ resistor.
5. One $260\,k\Omega$ resistor.

6. One $1\,M\Omega$ resistor.

7. One $5.6\,M\Omega$ resistor.

8. Additional resistors and capacitors you choose to match your circuit designs.

13.4 Procedure

13.4.1 The Voltage Clamper

In this section, we will be building and measuring the behavior of the voltage clamp sketched in Figure 13.11. We will use our DS335 to output voltages with amplitudes on the order of a few volts and a mid-range frequency such as $f = 1\,kHz$.

$$v_{in}(t) \quad = \quad v_0 \cos(\omega t)$$

where $v_0 \approx 1 - 5\,V$. Initially, we will choose $C = 1\mu F$ and take $R = 47\,k\Omega$ to build the circuit in Figure 13.11.

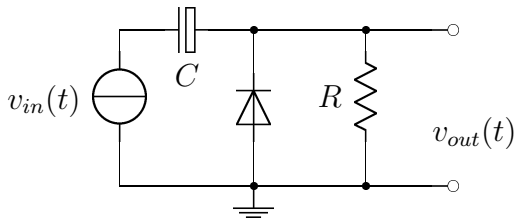

Figure 13.11: A voltage-clamper circuit.

Question 13.1 *With our choice of R and C, do we expect to be able to buffer the capacitor DC voltage? How quickly will the capacitor discharge compared to the period of the input voltage?*

1. Using an input voltage of $5\,V$ peak-to-peak, measure the output voltage across the resistor. Be sure to note the average DC level of this voltage and the amplitude of the AC component of the voltage?

2. Change the resistance to $100\,k\Omega$ and repeat your measurements.

3. Remove the resistor altogether and just make your measurements across the diode.

Question 13.2 *Assuming that you are using a* $47\,k\Omega$ *resistor, what do you expect to happen in part 1 if you use a much smaller capacitor, say* $0.01\,\mu F$*?*

13.4.2 The Voltage Doubler

The voltage-doubler circuit can be built by adding a second diode/capacitor stage to the voltage clamp in Section 13.1.1 as shown in Figure 13.12. In this circuit, we will take both capacitors to be $1\,\mu F$ and the diodes will be 1N4004s. We will choose various resistors and then examine the average DC level and the AC ripple amplitude at the output.

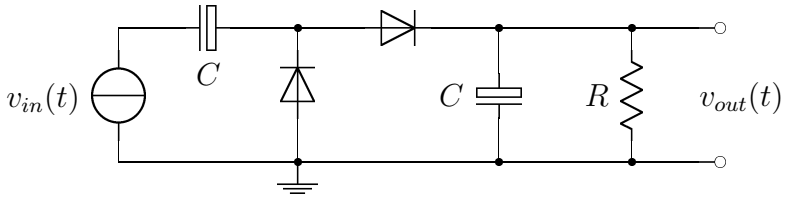

Figure 13.12: The voltage-doubler circuit.

1. Build the circuit shown in Figure 13.12. Using an input AC signal with a frequency of $1000\,Hz$ and a peak-to-peak amplitude of $5\,V$, measure both the average voltage (DC level) and the amplitude of the voltage ripple for an open circuit (no resistor).

2. Measure the average voltage and ripple voltage with several different values of R ranging from $47\,k\Omega$ up to $5.6\,M\Omega$.

Question 13.3 *For the* $1\,kHz$ *signal that you used, what is the output impedance,* $\mid Z_{out} \mid$ *of your voltage doubler? How does this compare to the impedance of one of our capacitors?*

3. Using your $260\,k\Omega$ resistor, measure the average voltage and ripple voltage for input frequencies of $1\,kHz$, $5\,kHz$, $10\,kHz$ and $50\,kHz$.

Question 13.4 *Do you see the expected frequency response of the output voltage?*

13.4.3 The Voltage Multiplier

We will now continue to add multiplication stages to our circuit in Figure 13.12 until we reach the three-stage multipler shown in Figure 13.13. As we did earlier, we will continue to use 1N4004 diodes and $1\,\mu F$ capacitors. We are interested in characterizing the behavior of this circuit for an input signal

$$v_{in}(t) \quad = \quad v_0 \cos(2\pi f t) \ ,$$

where v_0 is $5.0\,V$ and f is $1\,kHz$.

1 Build the voltage-multiplier circuit as shown in Figure 13.13. As with the doubler circuit, use the assortment of resistors from $47, k\Omega$ to $5.6\,M\Omega$ to characterize the average voltage and the ripple voltage for a $1\,kHz$ input frequency.

2 Determine the output impedance of the multiplier.

3 Repeat your measurements using a $5\,kHz$ and $10\,kHz$ input frequency. Characterize the output impedance for both of these frequencies.

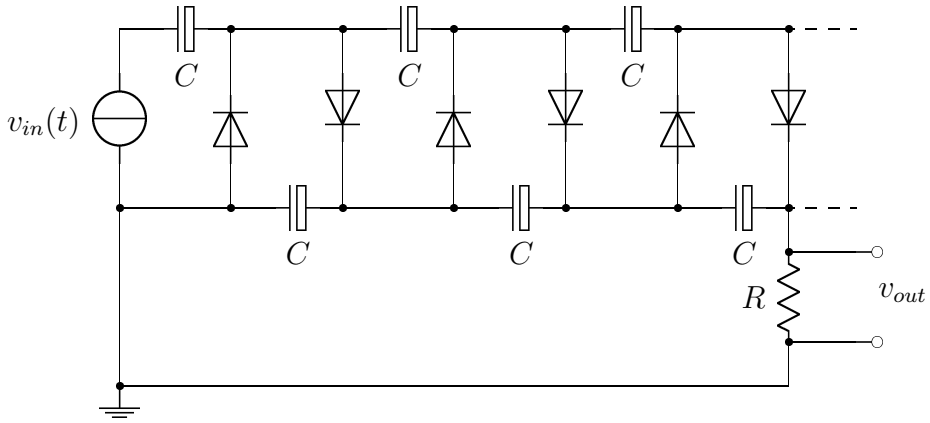

Figure 13.13: The voltage multiplier.

Question 13.5 *If would like to be able to drive a* $260\,k\Omega$ *load with our multiplier and have the ripple voltage smaller than* $1\,mV$*, estimate the minium frequency we need to operate at?*

Question 13.6 *What would happen if we used a smaller capacitor such as* $0.1\,\mu F$*?*